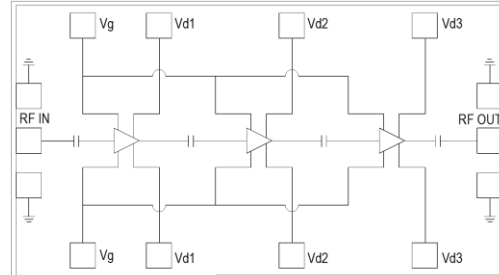


## 8 – 12GHz 12 Watt High Power Amplifier

### Features

- ◆ Frequency Range: 8 – 12GHz
- ◆ 41dBm Saturated Pulsed Output Power
- ◆ 25dB Small Signal Gain
- ◆ 35% PAE
- ◆ DC decoupled input and output
- ◆ Dual sided bias supply
- ◆ Chip dimension: 4.8 x 4.1 x 0.1 mm

### Functional Diagram



### Typical Applications

- ◆ RADAR
- ◆ Military & Space
- ◆ LMDS, VSAT

### Description

The ASL4048 is X-band Power amplifier operates in 8 – 12GHz frequency range with 12W saturated output power over entire bandwidth. The PA uses 3 stages of amplification featuring 25dB of Small Signal Gain with input & output return losses better than 10dB and 35% PAE over the operating frequency. The chip operates with dual bias supply voltage. The die is fabricated using a reliable 0.25 $\mu$ m InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

### Absolute Maximum Ratings <sup>(1)</sup>

Parameter	Absolute Maximum	Units
Drain bias voltage ( $V_d=V_{d1}=V_{d2}=V_{d3}$ @ $I_{dq}=3.5A$ )	9.0	volts
Drain Current ( $I_d=I_{d1}+I_{d2}+I_{d3}$ ) @ $V_d=8.5V$	5.5	A
Gate Bias Voltage ( $V_g=V_{g1}=V_{g2}=V_{g3}$ )	$-2.2 \leq V_g \leq -0.6$	V
RF input power (RFIn @ $V_d=8.5V$ )	23	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

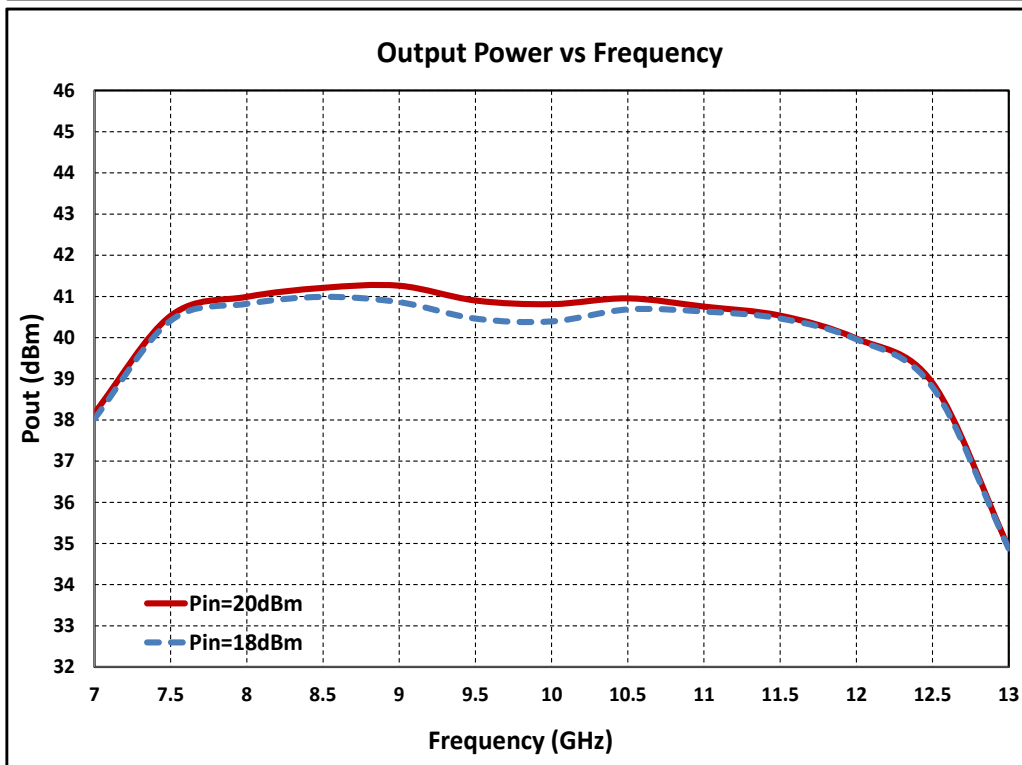
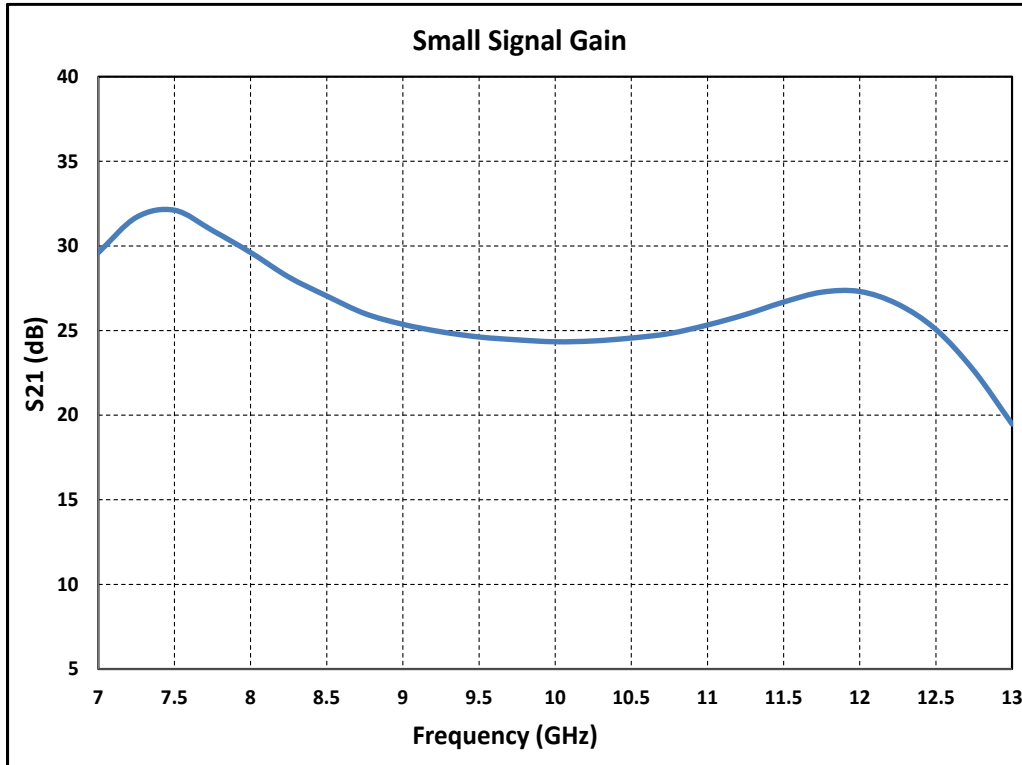
1. Operation beyond these limits may cause permanent damage to the component

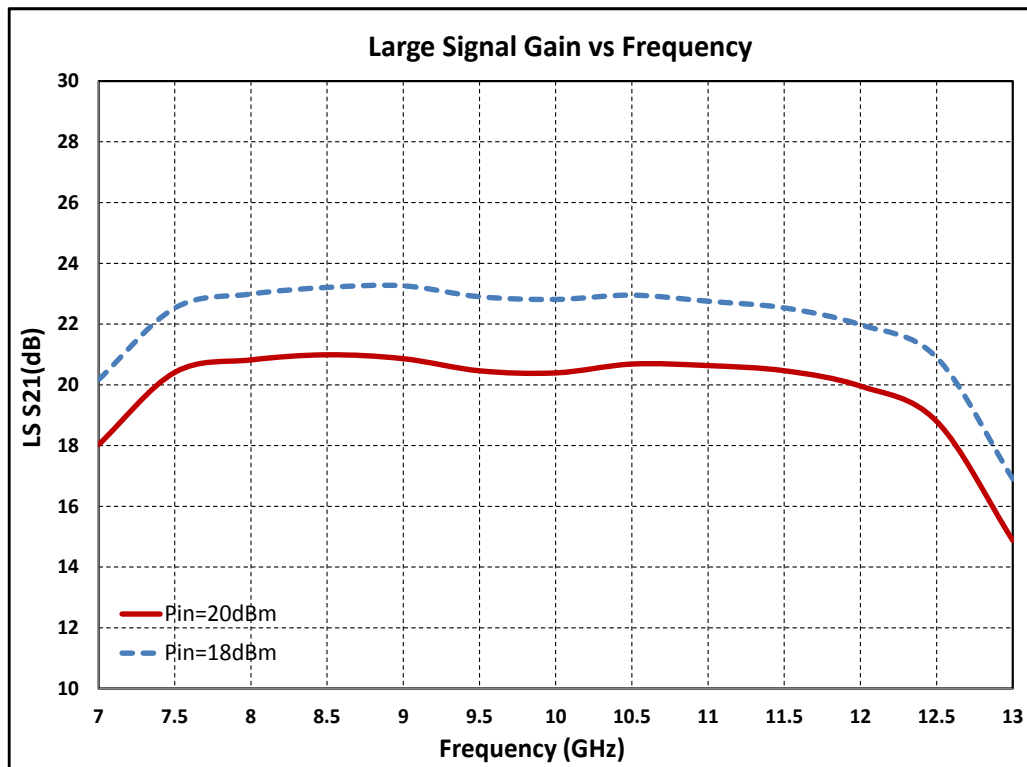
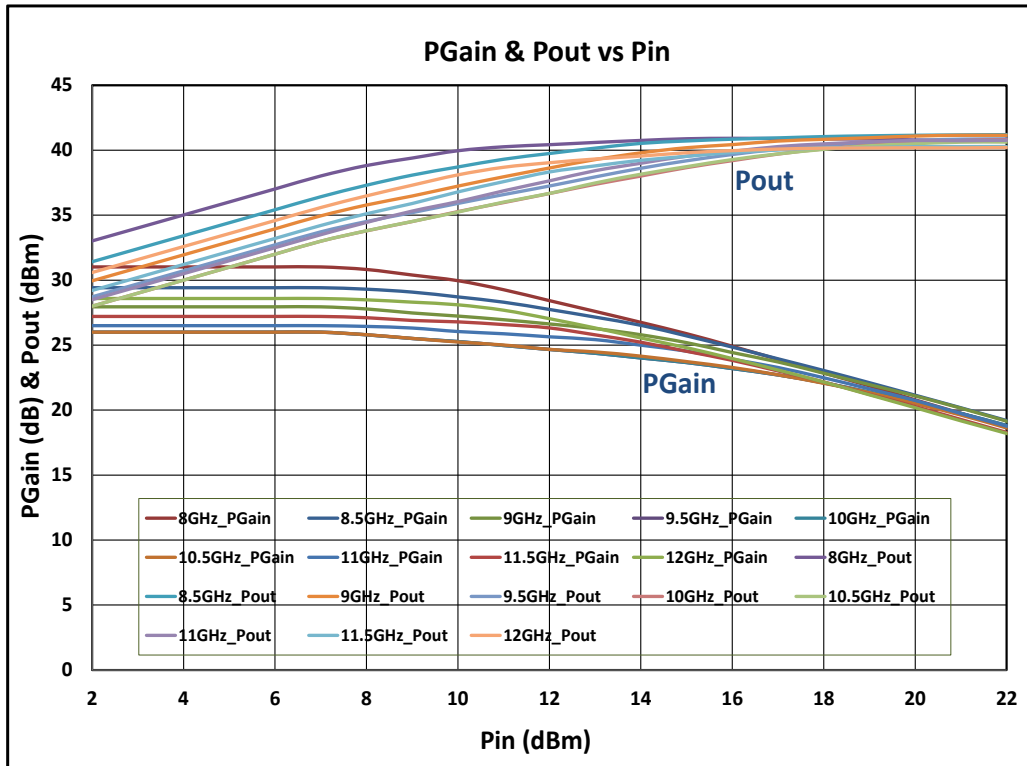
**Electrical Specifications <sup>(1)</sup> @  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{d1} = V_{d2} = V_{d3} = 8.5\text{V}$ ,  
 Total Current ( $I_{dq}$ ) =  $I_{dq1} + I_{dq2} + I_{dq3} = 3.5\text{A}$ ,  $Z_o = 50\Omega$ , Pulse Duty Cycle = 10%**

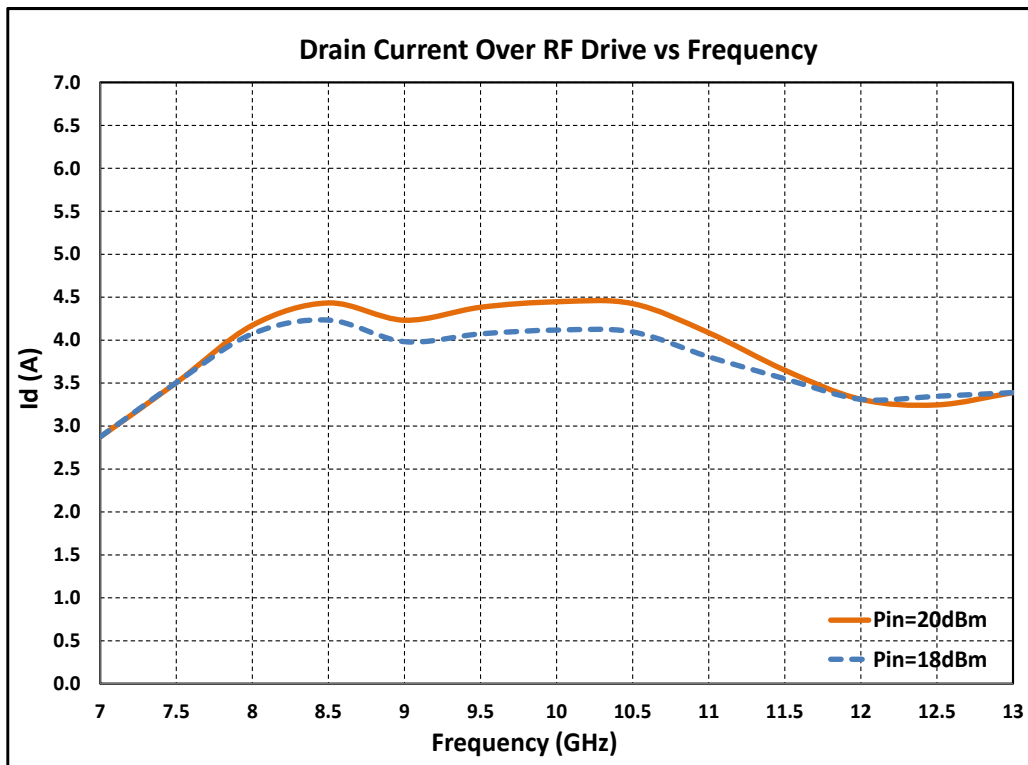
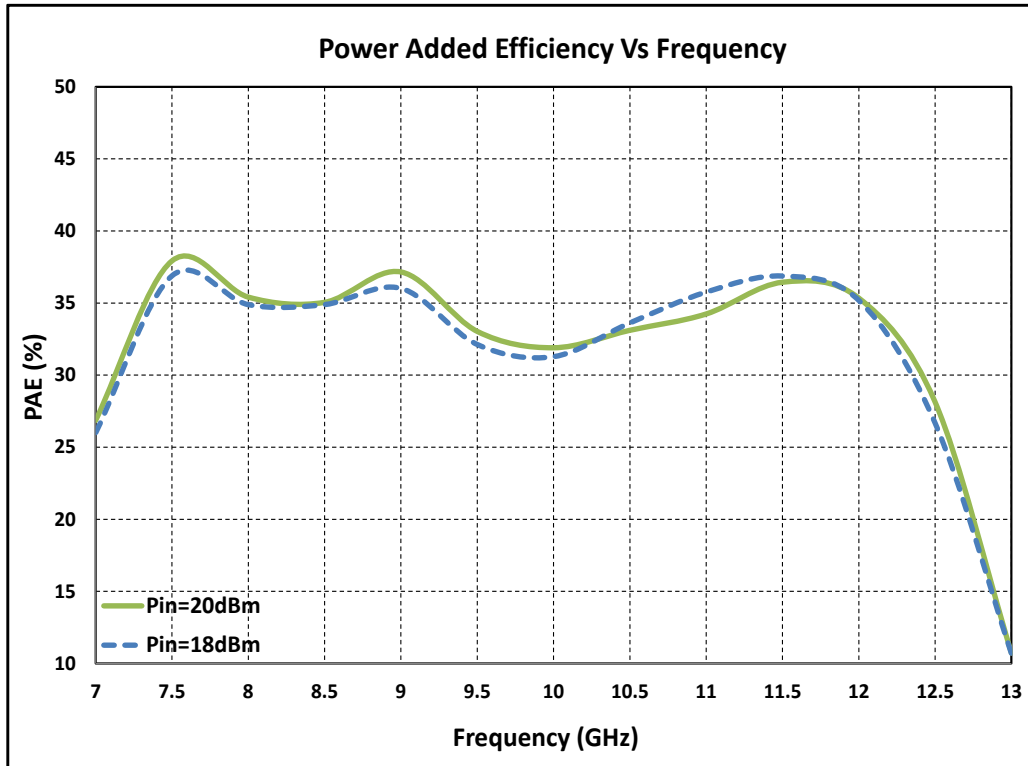
Parameter	Min.	Typ.	Max.	Units
Frequency Range	8	-	12	GHz
Small Signal Gain	22	25	-	dB
Gain Flatness	-	+/-2.5	-	dB
Large Signal Gain @ Pin = 18dBm	-	22	-	dB
Input Return Loss	-	<-10	-	dB
Output Return Loss	-	<-15	-	dB
Saturated output power (Psat)	-	12	-	W
Power Added Efficiency (PAE) <sup>2</sup>	-	35	-	%
Gate Voltage ( $V_g = V_{g1} = V_{g2} = V_{g3}$ ) <sup>4</sup>	-1	-0.75	-0.6	V
Supply Current ( $I_{dq}$ ) <sup>3</sup>	-	3.5	-	A

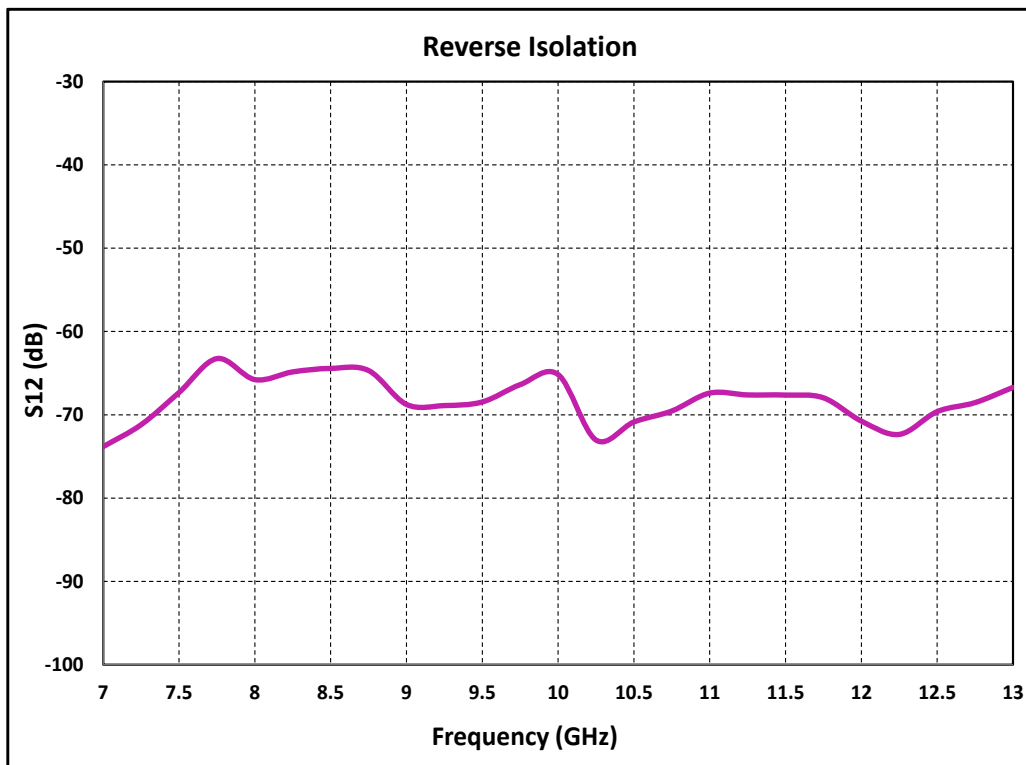
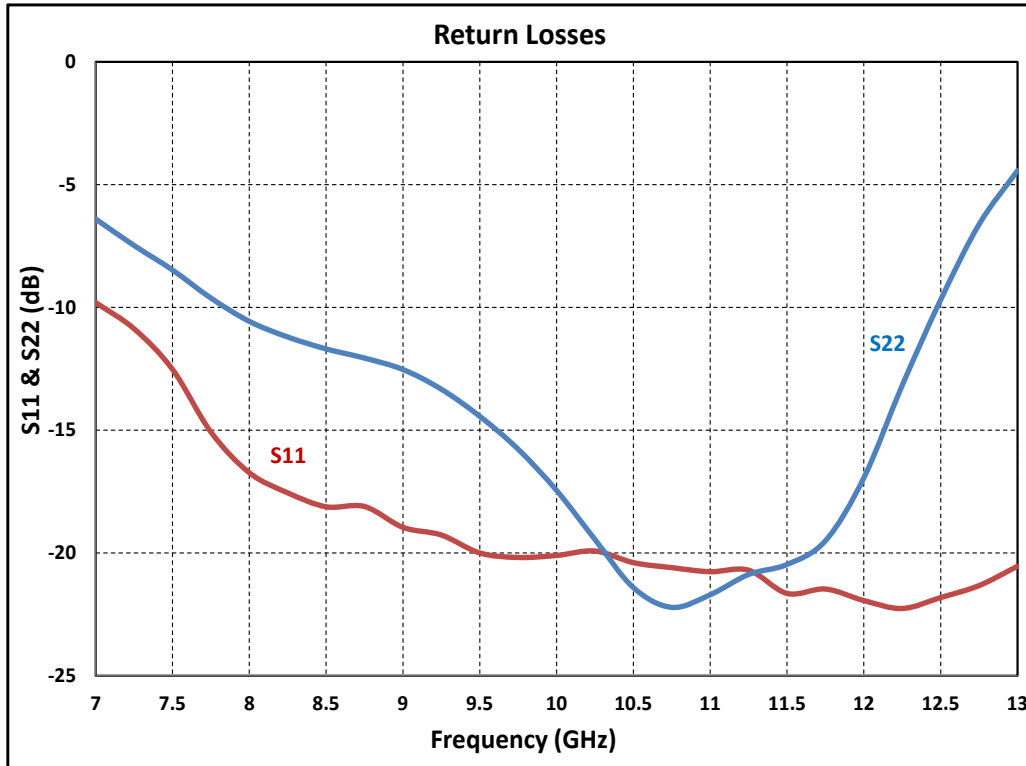
**Note:**

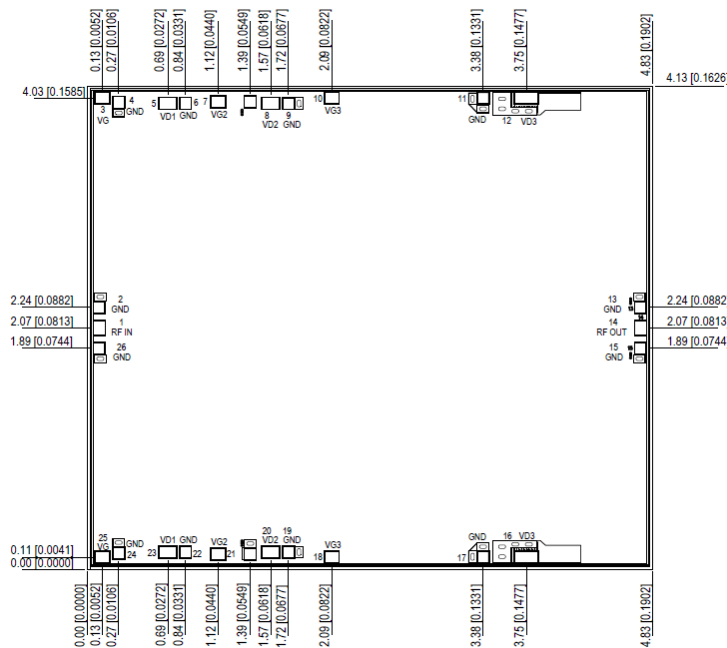
1. The above electrical specifications are on carrier measurements with 50 Ohms probes.
2. PAE is measured at 2dB Gain Compression Point.
3.  $I_{dq}$  - Drain Current under quiescent bias condition.
4. Gate Bias Voltage " $V_g$ " needs to be adjusted over the range mentioned in the above table in order to set the required quiescent current.

**On Carrier Measurements with 50 Ohms Probes:**
 $V_{d1}=V_{d2}=V_{d3}=8.5V$ , Total Current ( $I_{dq}$ ) = 3.5A,  $T_A=25\text{ }^\circ\text{C}$ , Pulse Duty Cycle=10%


**On Carrier Measurements with 50 Ohms Probes:**
 $V_{d1}=V_{d2}=V_{d3}=8.5V$ , Total Current ( $I_{dq}$ ) = 3.5A,  $T_A=25\text{ }^\circ\text{C}$ , Pulse Duty Cycle=10%


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**On Carrier Measurements with 50 Ohms Probes:** $V_{d1}=V_{d2}=V_{d3}=8.5V$ , Total Current ( $I_{dq}$ ) = 3.5A,  $T_A=25\text{ }^\circ\text{C}$ , Pulse Duty Cycle=10%

**Bond Pad Details:**


**Units:** millimeters (inches)

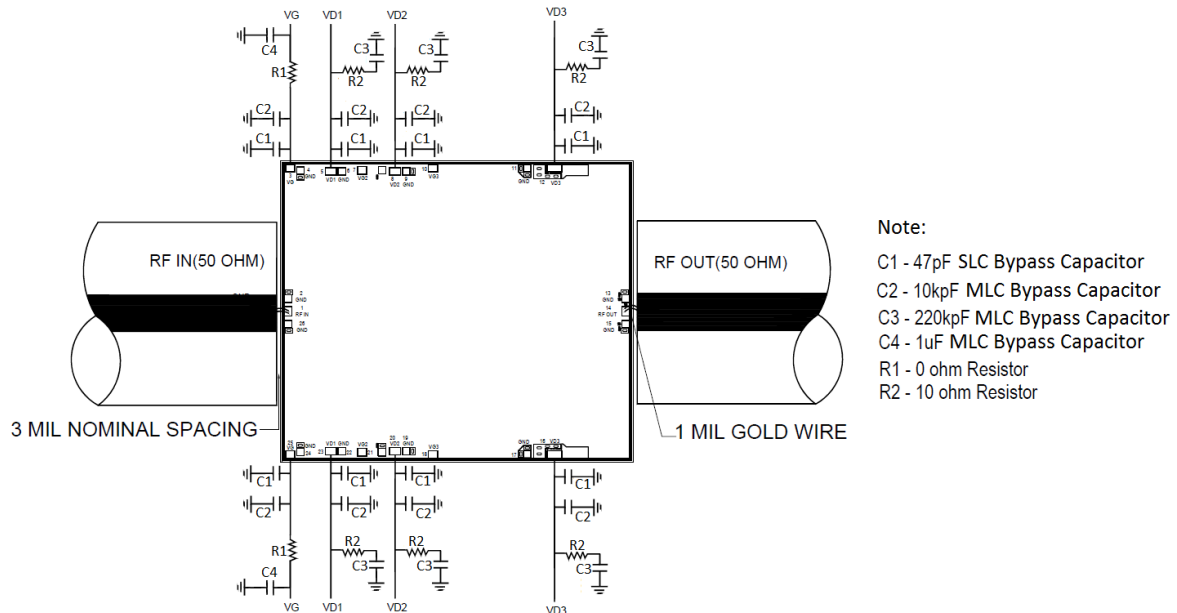
**Note:**

1. RF and DC bond pads are 100 $\mu$ m x 100 $\mu$ m
2. Pad no. 1 : RF IN
3. Pad no. 14 : RF Output
4. Pad no. 3,25 : Common Gate Voltage( $V_g$ )
5. Pad no. 5,23 : 1<sup>st</sup> stage drain Voltage( $V_{d1}$ )
6. Pad no. 7,21 : 2<sup>nd</sup> stage gate Voltage( $V_{g2}$ ) – No Connection
7. Pad no. 8,20 : 2<sup>nd</sup> stage drain Voltage ( $V_{d2}$ )
8. Pad no. 10,18 : 3<sup>rd</sup> stage gate Voltage( $V_{g3}$ ) – No Connection
9. Pad no. 12,16 : 3<sup>rd</sup> stage drain Voltage ( $V_{d3}$ )
10. Pad no. 2,4,6,9,11,13,15, 17,19,22,24 : GND

**Off Chip Components used for On Carrier Assembly:**

Component Name	Part Number/Description	Vendor
47pF SLC Capacitors	CAP DI SL 47PF $\pm$ 10% 50V - D20BJ470K5PX or Equivalent	DLI
10kpF MLC Capacitor	04023C103KAT2A $\pm$ 10%;25V or Equivalent	AVX Corp.
1uF MLC Capacitor	0402YC105KAT2A $\pm$ 10%;16V or Equivalent	AVX Corp.
0.22uF MLC Capacitor	0402YC224KAT2A $\pm$ 10%;16V or Equivalent	AVX Corp.

## Recommended Assembly Diagram



### Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output bondpads.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 47pF single layer bypass capacitors.
3. Input and output 50 ohm lines are preferably on 5 mil or 10 mil RT Duroid substrate.
4. 47pF single layer bypass capacitors mentioned above need to be placed at closest possible distance to the corresponding DC bond pads.
5. The RF input & output ports are DC decoupled on-chip.
6. This chip is not preferred to be operated under continuous DC voltages, unless it is applied with considerably low drain voltage level ( $V_d \leq 5V$ ).
7. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip.

**Die attach:** Eutectic attachment using flux less AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

**Wire bonding:** For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 to 200 $\mu$ m length of wedge bonds is advised. Single Ball bonds of 250-300 $\mu$ m though acceptable, may cause a deviation in RF performance.



**GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing**

All information and Specifications are subject to change without prior notice. Before using the product, please download and refer to latest datasheet from website.