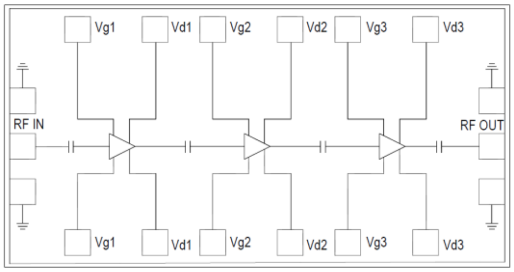
8 – 12GHz 10 Watt High Power Amplifier

Features

- **Frequency Range: 8 – 12GHz**
- **40 dBm Psat**
- **25 dB Small Signal Gain**
- **28% PAE**
- **High IP3**
- **DC decoupled input and output**
- **InGaAs pHEMT Technology**
- **Chip dimension: 4.8 x 4.1 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4039 is X-band Power amplifier operates in 8 – 12GHz frequency range with 40dBm output power over entire bandwidth. The PA uses 3 stages of amplification featuring 25 dB of Small Signal Gain with input & output return losses better than 10dB and 28% PAE over the operating frequency. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.25µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (V_d=V_{d1}=V_{d2}=V_{d3} @ I_{dq} = 3.5A)	+9	volts
Drain Current (I_d=I_{d1}+I_{d2}+I_{d3}) at V_d=8.5V	5.5	A
Gate Bias Voltage (V_g=V_{g1}=V_{g2}=V_{g3})	$-2.2 < V_g < -0.6$	V
RF input power (RFin at V_d=8.5V)	23	dBm
Operating temperature	-50 to +85	^oC
Storage Temperature	-65 to +150	^oC

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications $^{(1)}$ @ $T_A = 25\ ^oC$, $V_d = V_{d1} = V_{d2} = V_{d3} = 8.5V$, *Total Current* ($I_{dq}$) = $I_{dq1}+I_{dq2}+I_{dq3} = 3.5A$, $Z_o = 50\ \Omega$, Pulse Duty Cycle = 10%

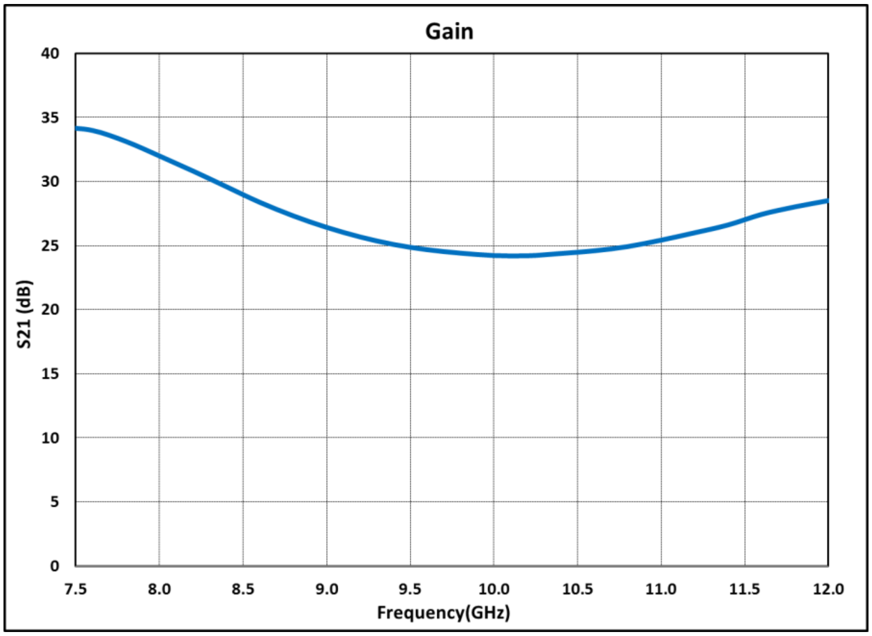
Parameter	Min.	Typ.	Max.	Units
Frequency Range	8		12	GHz
Small Signal Gain	-	25	-	dB
Gain Flatness	-	+/-3	-	dB
Input Return Loss	-	<-10	-	dB
Output Return Loss	-	<-15	-	dB
Saturated output power (Psat)	-	40	-	dBm
Power Added Efficiency (PAE)[2]	-	28%	-	-
Gate Voltage (V_g=V_{g1}=V_{g2}=V_{g3})[3]	-1	-0.75	-0.6	V
Supply Current(I_{dq})	-	3.5	-	A

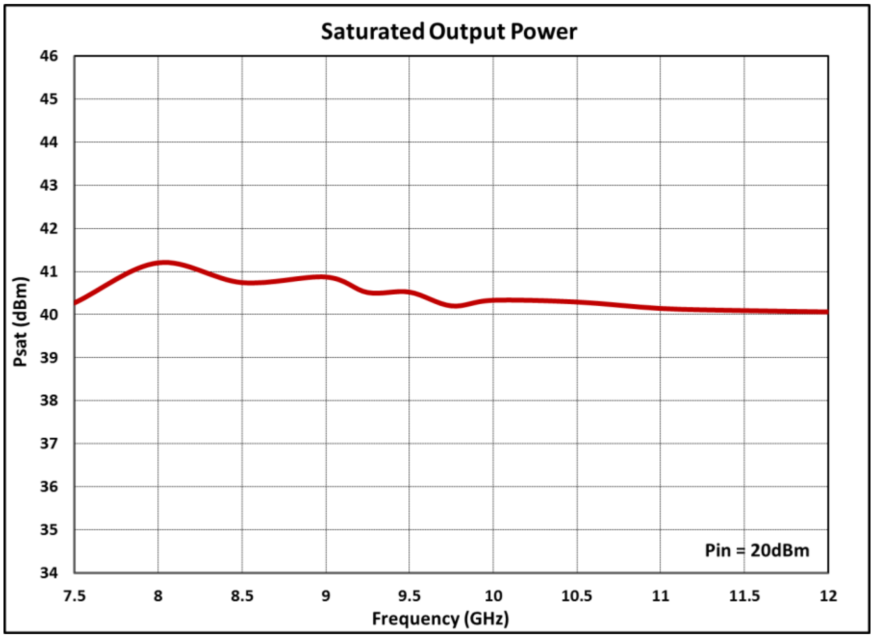
Note:

1. The above electrical specifications are on carrier measurements with 50 Ohms probes.
2. PAE is measured at 2dB Gain Compression Point.
3. Gate Bias Voltage “V_g” needs to be adjusted over the range mentioned in the above table in order to set the required value of “I_{dq}”.

On Carrier Measurements with 50 Ohms Probes:

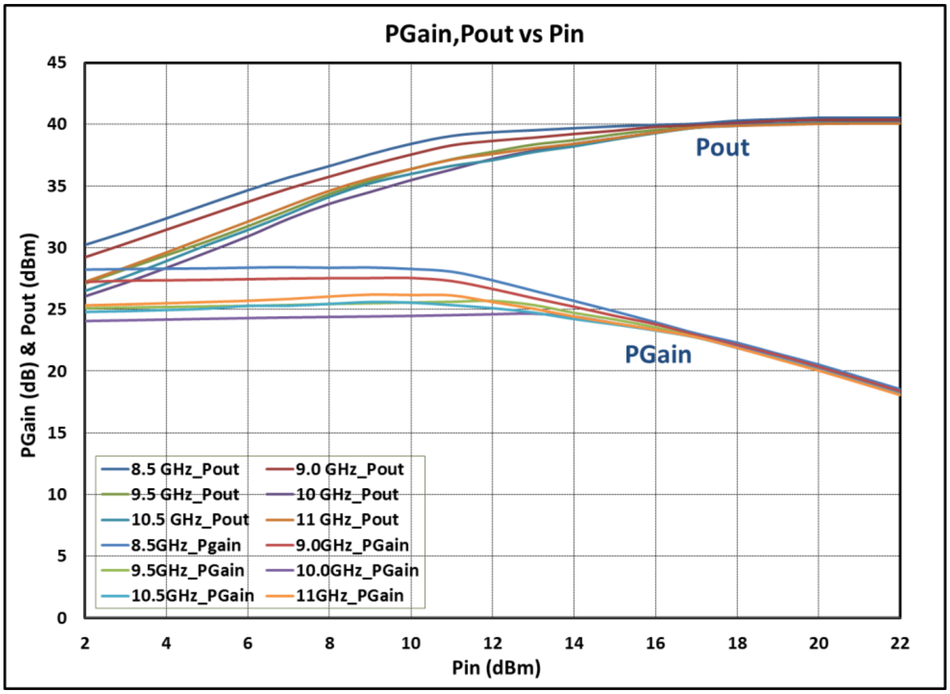
V_{d1}=V_{d2}=V_{d3}=8.5V, *Total Current (I_{dq})=3.5A, T_A=25 ^{o}C, Pulse Duty Cycle=10%*

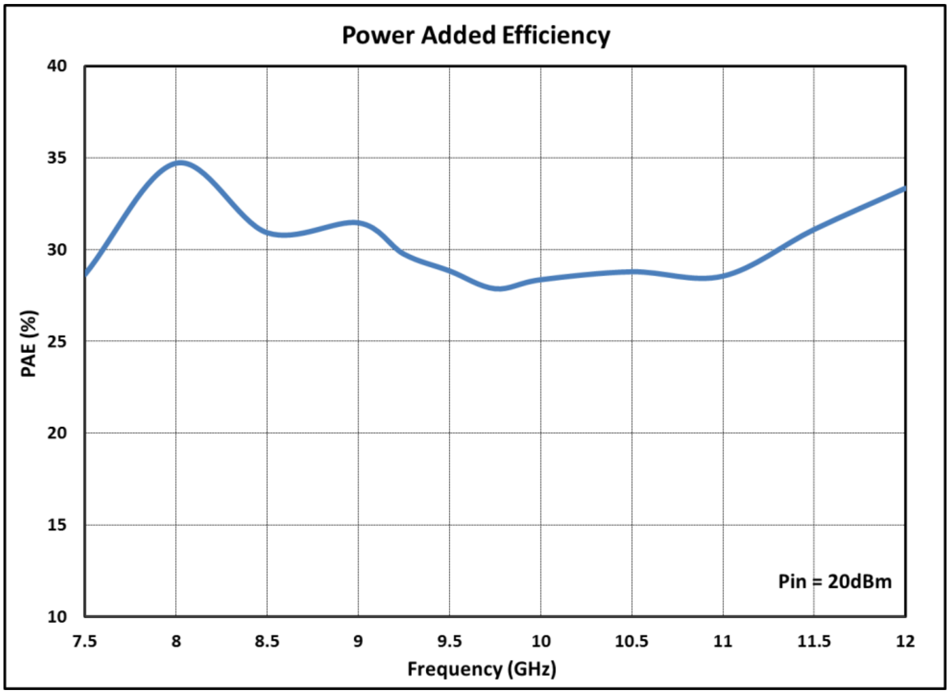




On Carrier Measurements with 50 Ohms Probes:

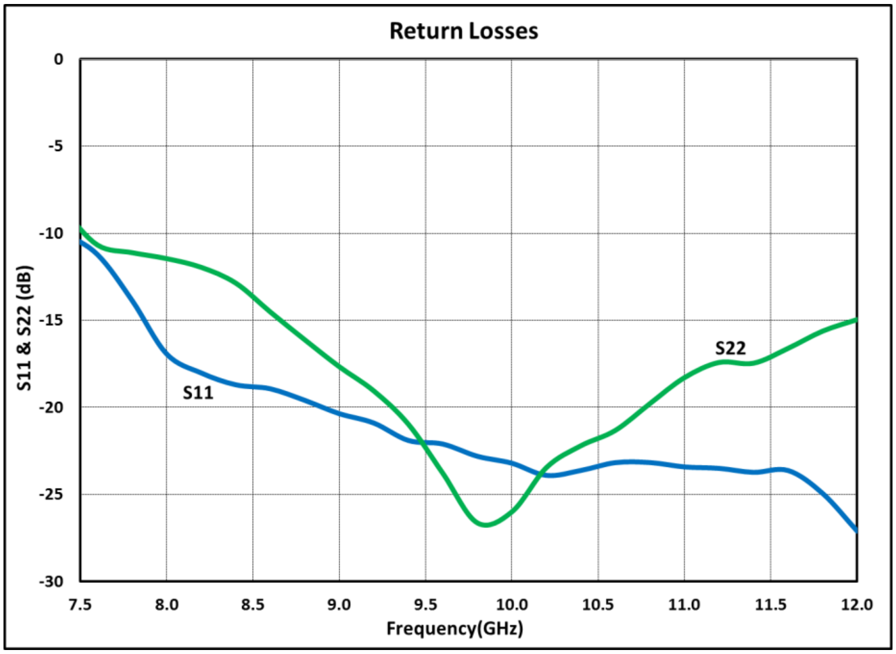
$V_{d1}=V_{d2}=V_{d3}=8.5V$, *Total Current* ($I_{dq}$)*=3.5A*, $T_A=25\ ^oC$, *Pulse Duty Cycle=10%*

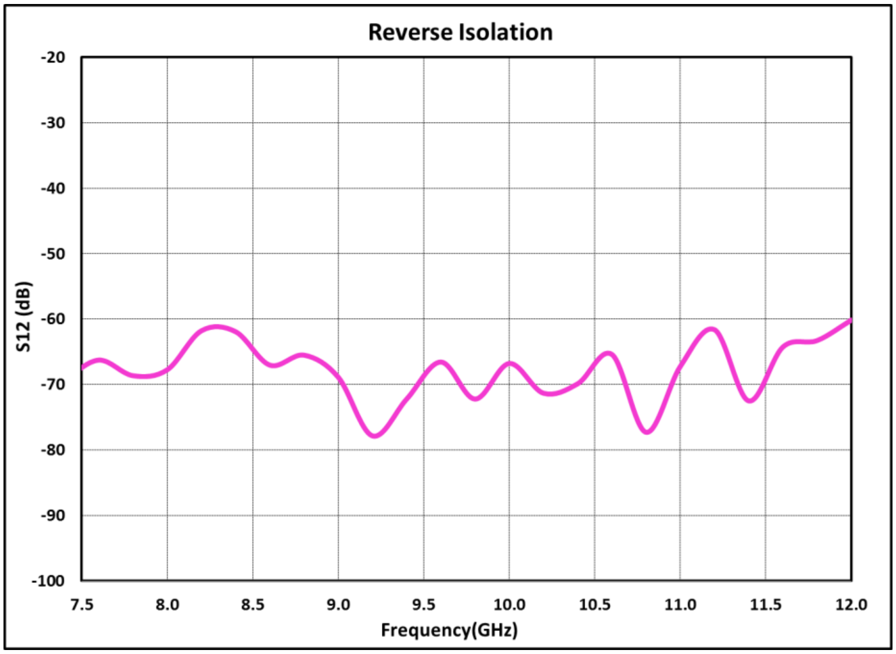




On Carrier Measurements with 50 Ohms Probes:

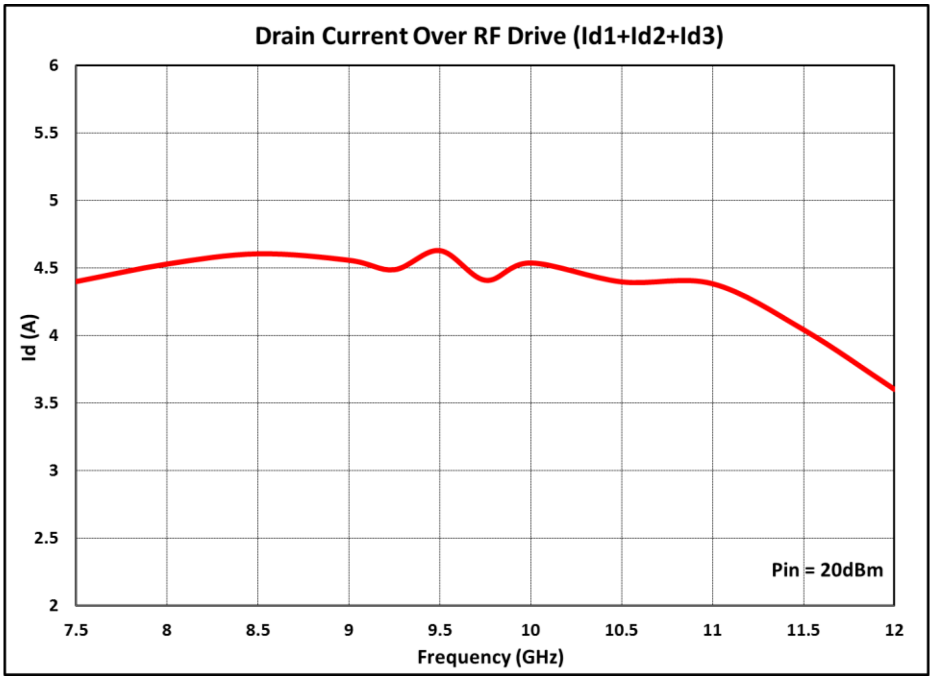
$V_{d1}=V_{d2}=V_{d3}=8.5V$, *Total Current* $(I_{dq})=3.5A$, $T_A=25\,^{o}C$, *Pulse Duty Cycle=10%*



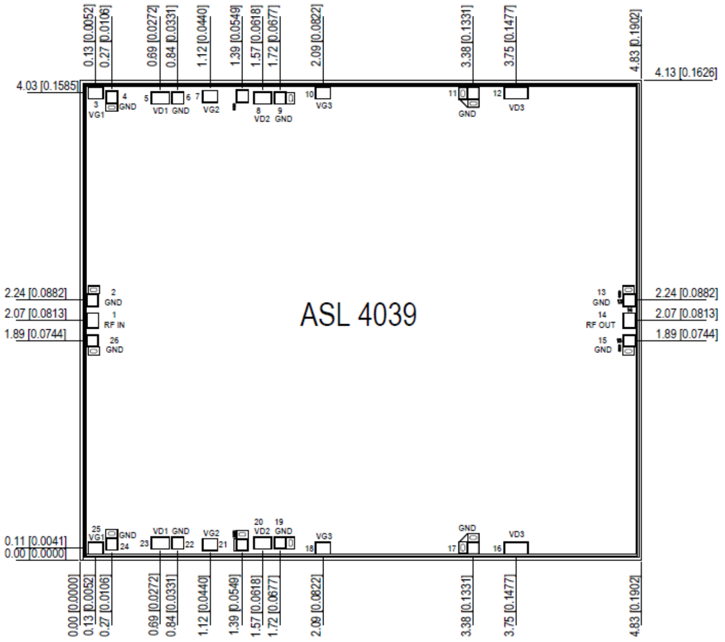


On Carrier Measurements with 50 Ohms Probes:

$V_{d1}=V_{d2}=V_{d3}=8.5V$, *Total Current* $(I_{dq})=3.5A$, $T_A=25\ ^oC$, *Pulse Duty Cycle=10%*



Bond Pad Details:



Units: millimeters (inches)

Note:

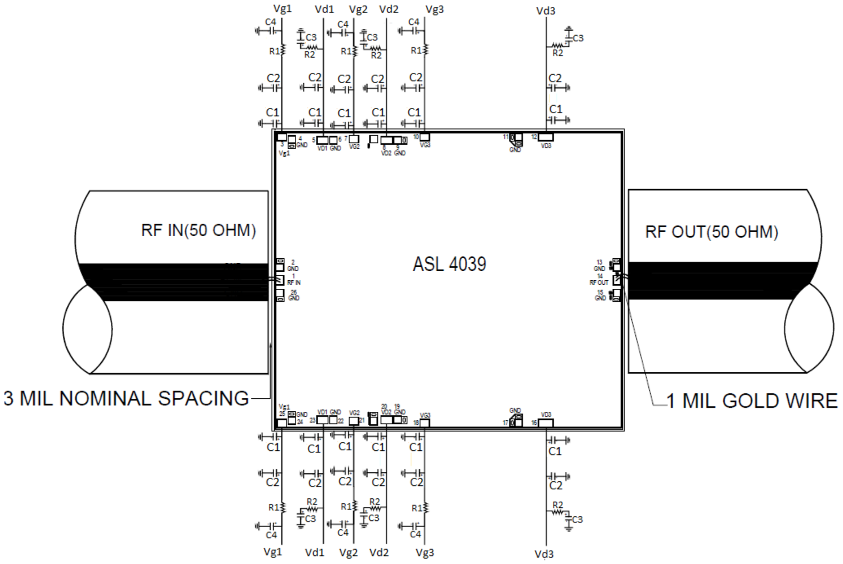
1. RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 14 : RF Output
4. Pad no. 3,25 : 1st stage gate voltage(V_{g1})
5. Pad no. 5,23 : 1st stage drain voltage(V_{d1})
6. Pad no. 7,21 : 2nd stage gate voltage(V_{g2})
7. Pad no. 8,20 : 2nd stage drain voltage (V_{d2})
8. Pad no. 10,18 : 3rd stage gate voltage(V_{g3})
9. Pad no. 12,16 : 3rd stage drain voltage (V_{d3})
10. Pad no. 2,4,6,9,11,13,15,
    17,19,22,24 : GND

    All the dimensions shown above are measured taking bottom left corner as reference.

Off Chip Components used for On Carrier Assembly:

Component Name	Part Number/Description	Vendor
47pF SLC Capacitors (C1)	CAP DI SL 47PF±10% 50V - D20BJ470K5PX or Equivalent	DLI
10kpF MLC Capacitor (C2)	04023C103KAT2A±10%;25V or Equivalent	AVX Corp.
1uF MLC Capacitor (C4)	0402YC105KAT2A±10%;16V or Equivalent	AVX Corp.
220kpF MLC Capacitor (C3)	0402YC224KAT2A±10%;16V or Equivalent	AVX Corp.

Recommended Assembly Diagram



Note:

C1 - 47pF SLC Bypass Capacitor
C2 - 10kpF MLC Bypass Capacitor
C3 - 220kpF MLC Bypass Capacitor
C4 - 1uF MLC Bypass Capacitor
R1 - 0 ohm Resistor
R2 - 10 ohm Resistor

Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 47pF single layer bypass capacitors.
3. Input and output 50 ohm lines are preferably on 5 mil RT Duroid substrate.
4. 47pF single layer bypass capacitors mentioned above need to be placed at closest possible distance to the corresponding DC bond pads.
5. The RF input & output ports are DC decoupled on-chip.
6. This chip is not preferred to be operated under continuous DC voltages, unless it is applied with considerably low drain voltage level ($V_d \leq 5V$).
7. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip.

Die attach: Eutectic attachment using flux less AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 to 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice. Before using the product, please download and refer to latest datasheet from website.