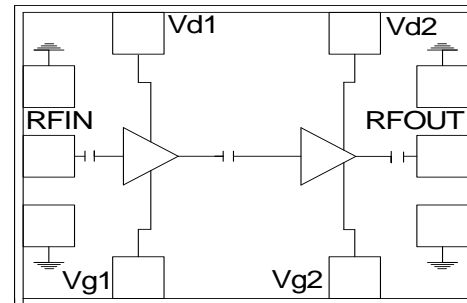


8.5 - 11 GHz Medium Power Amplifier

Features

- ◆ Frequency Range : 8.5 - 11GHz
- ◆ 20 dBm output Psat
- ◆ 20 dB Power Gain
- ◆ 25% PAE
- ◆ High IP3
- ◆ Input Return Loss > 8 dB
- ◆ Output Return Loss > 12 dB
- ◆ Dual bias operation
- ◆ No external matching required
- ◆ DC decoupled input and output
- ◆ 0.5 μ m InGaAs pHEMT Technology
- ◆ Chip dimension: 1.7 x 1.7 x 0.1 mm

Functional Diagram



Typical Applications

- ◆ RADAR
- ◆ Military & space
- ◆ LMDS, VSAT

Description

The ASL4032 is a X-band Medium Power Amplifier with 20dBm power output. The MPA uses 2 stages of amplification and operates in 8.5 - 11 GHz frequency range. The MPA features 20dB of gain with input and output return losses of 8dB and 12dB respectively. The MPA has a high IP3 of 30dBm and 25% PAE. The chip operates with dual bias supply voltage. The die is fabricated using a reliable 0.5 μ m InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings ⁽¹⁾

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+9.0	volts
Drain current (Idq)	120	mA
RF input power (RFin at Vd=9V)	20	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

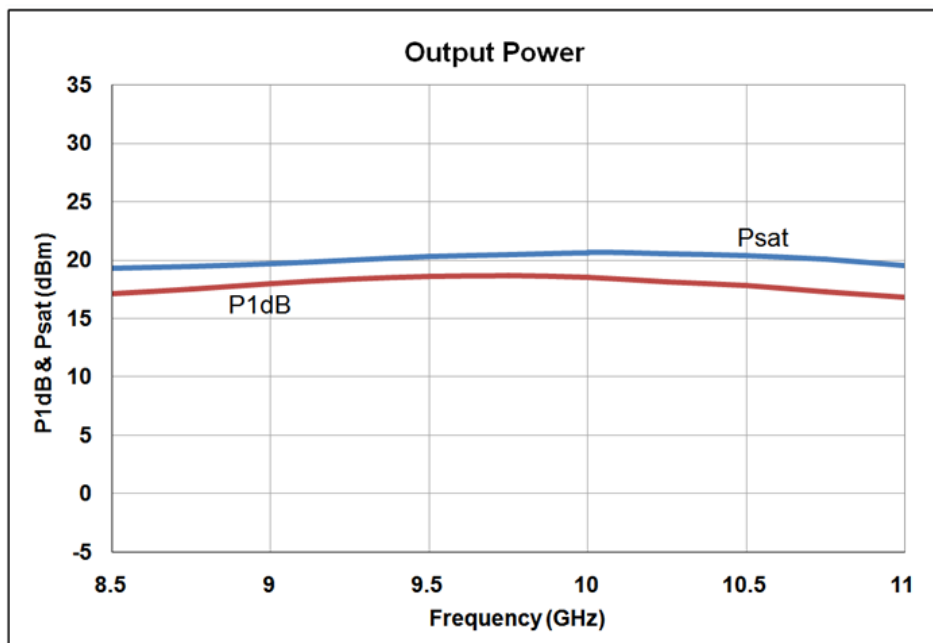
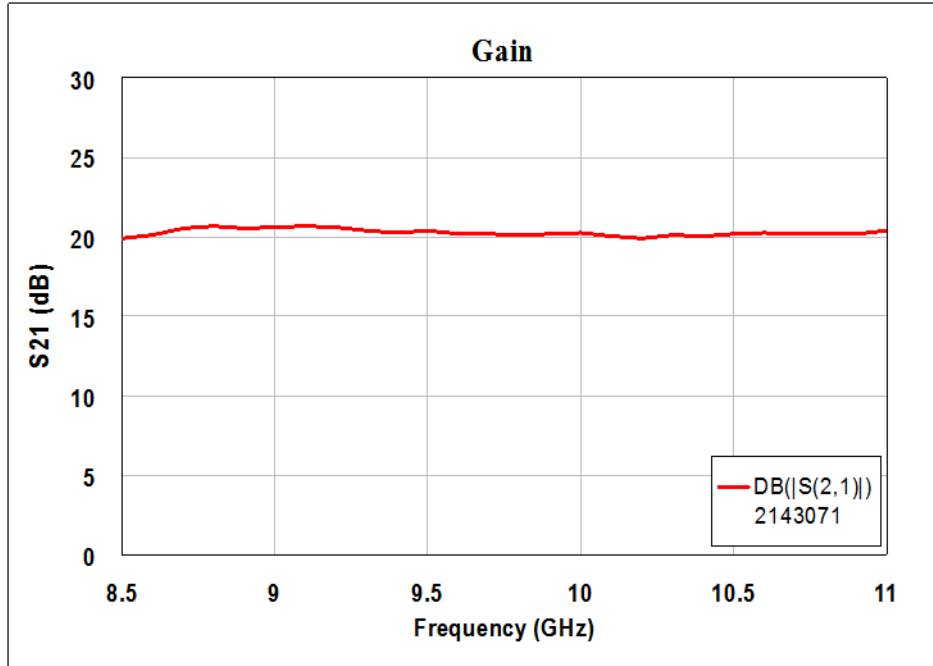
1. Operation beyond these limits may cause permanent damage to the component

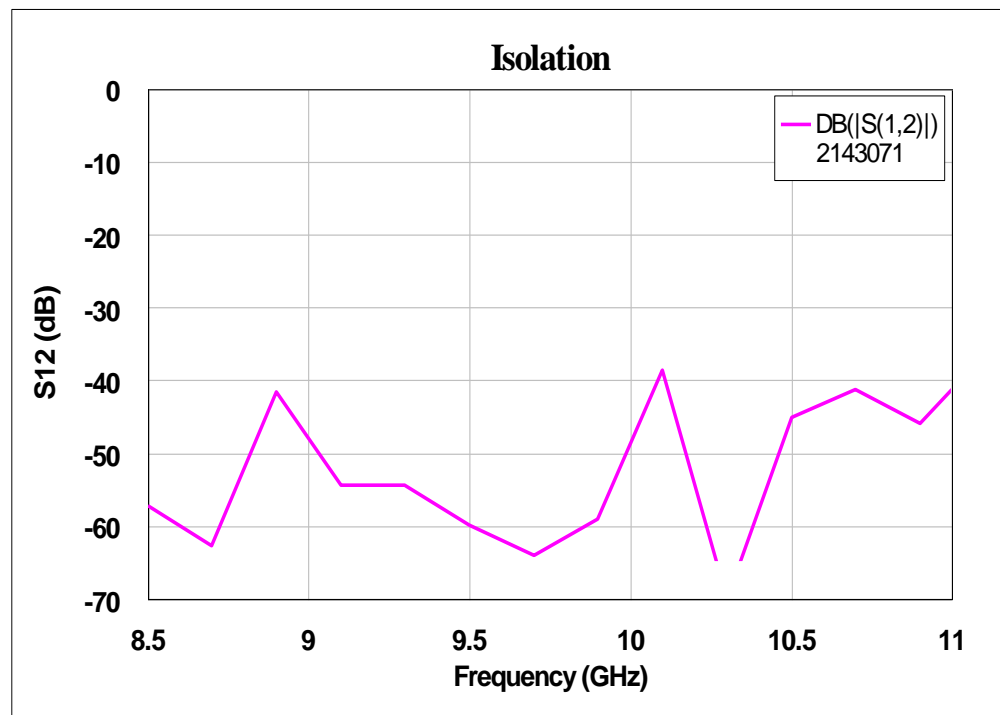
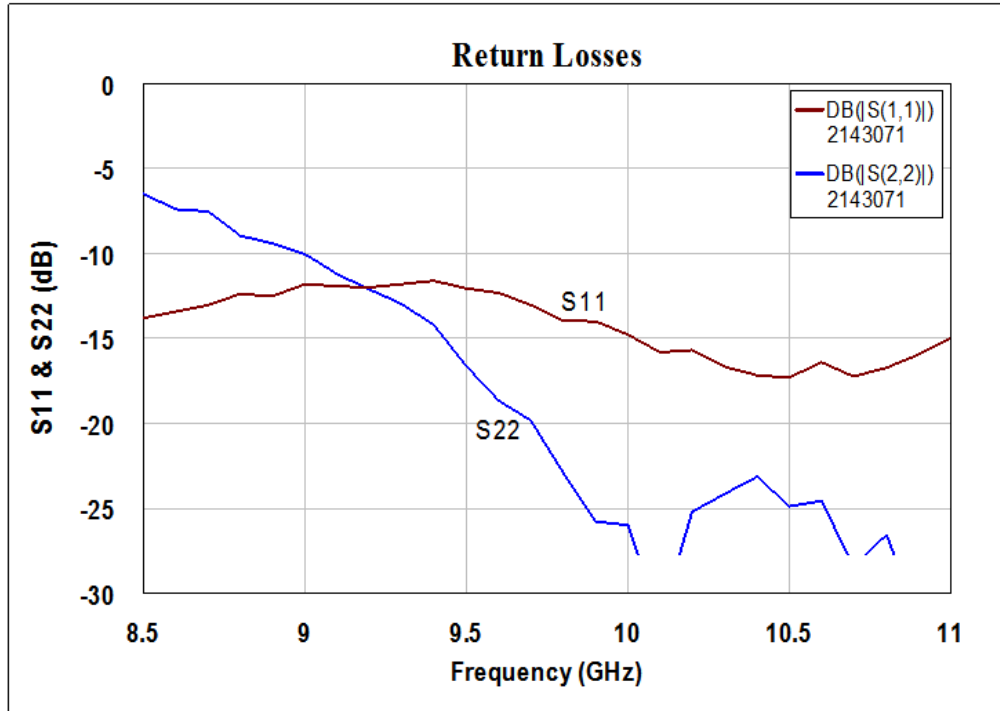
Electrical Specifications ⁽¹⁾ @ T_A = 25 °C, V_d = 5V, V_g = -0.9V, Z_o = 50 Ω

Parameter	Min.	Typ.	Max.	Units
Frequency Range	8.5 - 11	8.5 - 11	8.5 - 11	GHz
Gain	18	20		dB
Gain Flatness		+/-0.5		dB
Output Power (P1 dB)	17.5	18.5		dBm
Input Return Loss	6.5	8		dB
Output Return Loss	10	12		dB
Saturated output power (Psat)	19	20		dBm
Output Third Order Intercept (IP3)		30		dBm
Power Added Efficiency (PAE)		25%		--
Supply Current (Idq)		55		mA

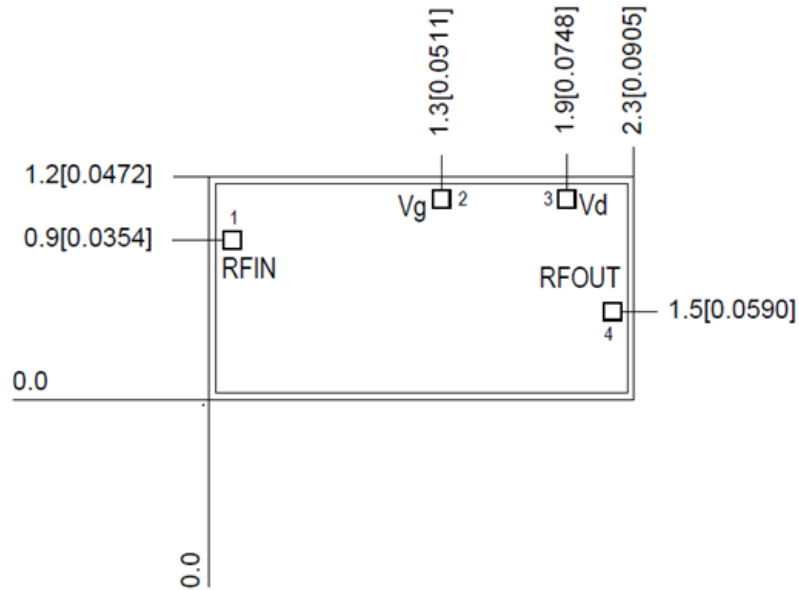
Note:

1. Electrical specifications as measured in test fixture.

Test fixture data
 $V_d = 5V, V_g = -0.9V, \text{Total Current } (I_{dq}) = 55mA, T_A = 25^\circ C$


Test fixture data
 $V_d = 5V, V_g = -0.9V, \text{Total Current } (I_{dq}) = 55mA, T_A = 25^\circ C$


Bond Pad Locations

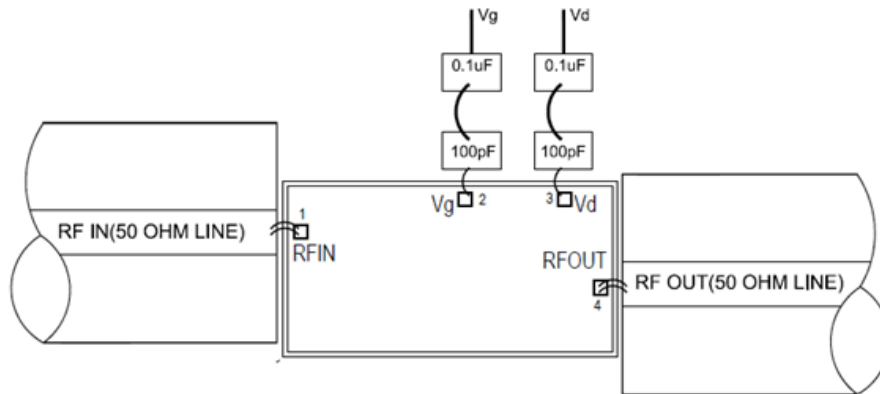


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100 μ m x 100 μ m
2. Pad no. 1 : RF IN
3. Pad no. 2 : Common gate voltage(V_g)
4. Pad no. 3 : Common drain voltage(V_d)
5. Pad no. 4 : RF OUT

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF Single Layer Bypass Capacitors
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 0.1 μ F capacitors may be additionally used as a second level of bypass for reliable operation
5. The RF input & output ports are DC decoupled on-chip

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200 μ m length of wedge bonds is advised. Single Ball bonds of 250-300 μ m though acceptable, may cause a deviation in RF performance.



GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice