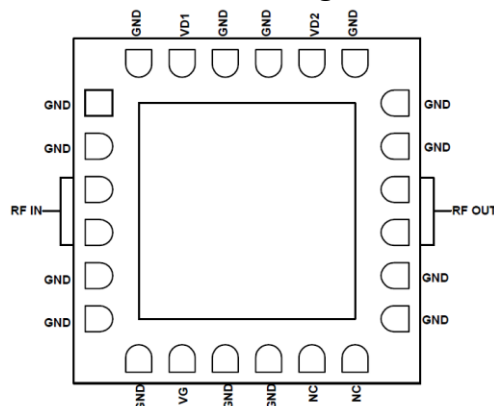


X Band 1W Power Amplifier

Features

- ◆ Frequency Range: 8.5 – 10.5GHz
- ◆ 30dBm output Psat
- ◆ 15 dB Gain
- ◆ 30% PAE
- ◆ Dual bias operation
- ◆ No external matching required
- ◆ DC decoupled input and output
- ◆ 4mm SQ QFN Package

Functional Diagram



Typical Applications

- ◆ RADAR
- ◆ Military & space
- ◆ LMDS, VSAT

Description

The ASL4018P4 is a X-band Power amplifier packaged in 4mm SQ. Ceramic QFN package with 1Watt Saturated Output Power. The PA uses 2 stages of amplification and operates over 8.5 – 10.5GHz frequency range. It features 15dB of Small Signal Gain with I/O return loss better than 8dB. It has a high IP3 of 38dBm and 30% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. It is fabricated using a reliable InGaAs pHEMT technology.

Absolute Maximum Ratings (Not Simultaneous) ⁽¹⁾

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+9	volts
Drain current (Id)	0.5	A
RF input power (RFin at Vd=8V)	25	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component.

Electrical Specifications ⁽¹⁾ @ T_A = 25°C, V_D = 8V, V_g = -1V, Z_o = 50 Ω

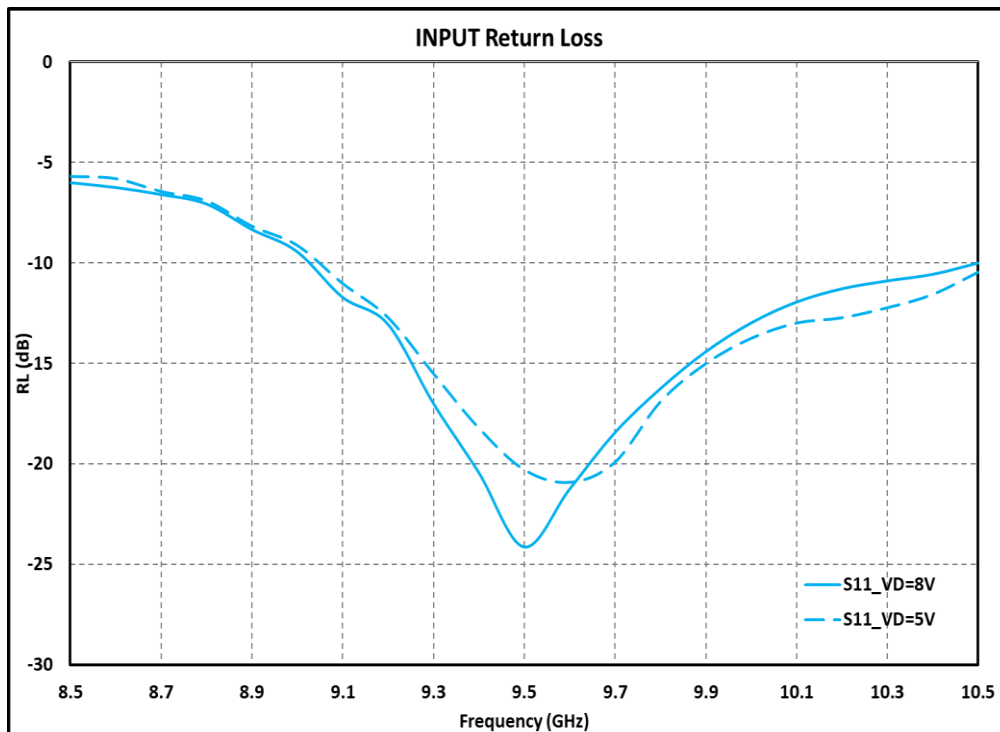
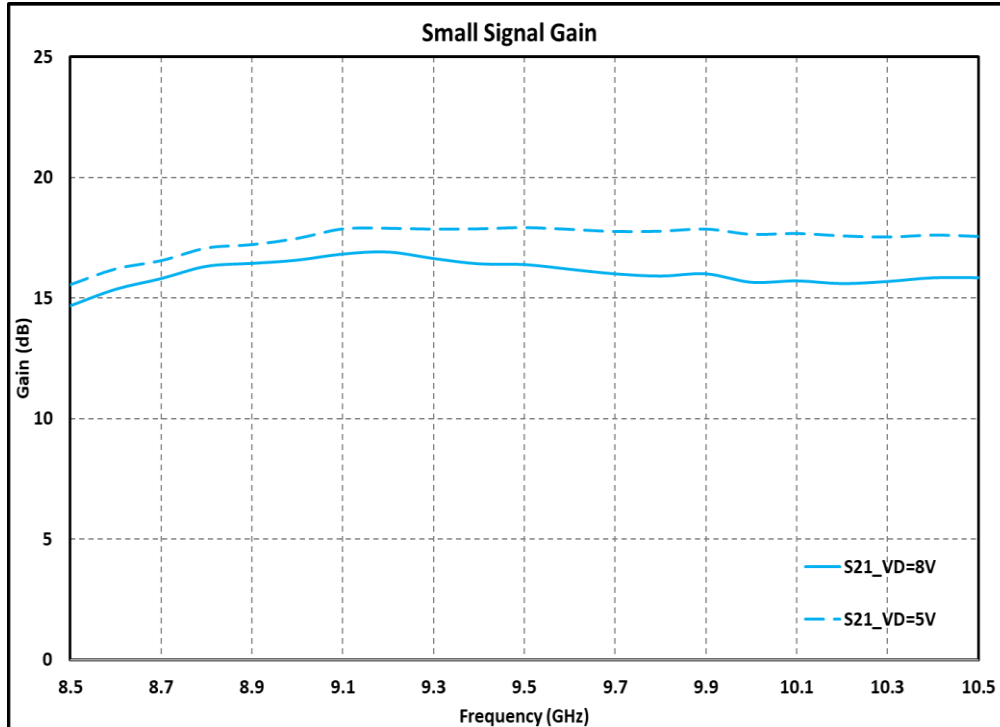
Parameter	Min.	Typ.	Max.	Units
Frequency Range	8.5		10.5	GHz
Gain	14	15		dB
Gain Flatness		+/-0.75		dB
Input Return Loss		-8		dB
Output Return Loss		-12		dB
Output Power (P ₁ dB)	29	30		dBm
Saturated output power (P _{sat})	29	31		dBm
Power Added Efficiency (PAE)	20	30		%
Drain Voltage (V _d)		8		V
Gate Voltage (V _g)	-1.4	-1	-0.7	V
Supply Current (I _{dq})		370		mA
Supply Current (I _{dsat})		400		mA

Note:

1. Electrical specifications as measured in test fixture.
2. T_A – Ambient Temperature;
3. I_{dsat} - Drain Current at Saturated Output Power

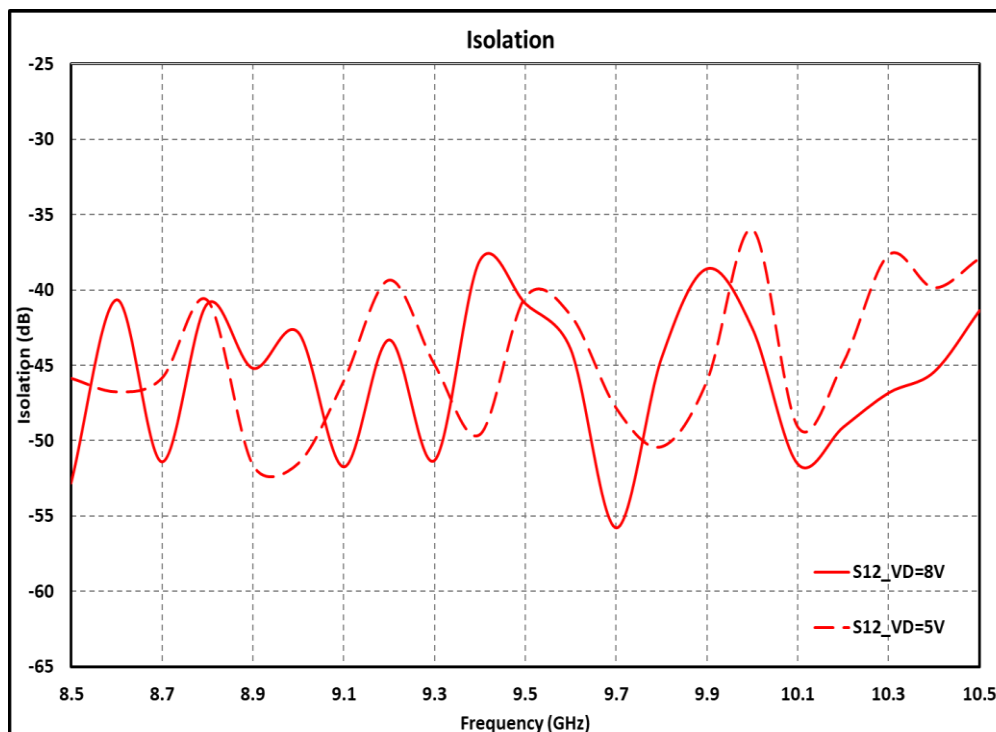
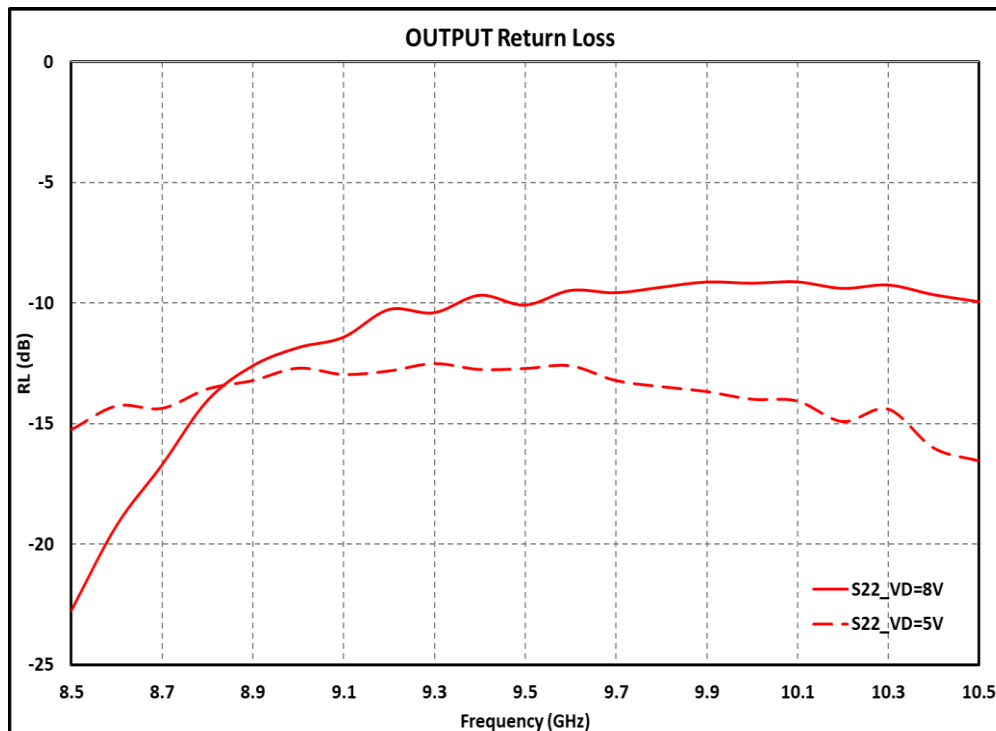
Test fixture data

$V_{d1} = V_{d2} = V_d$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



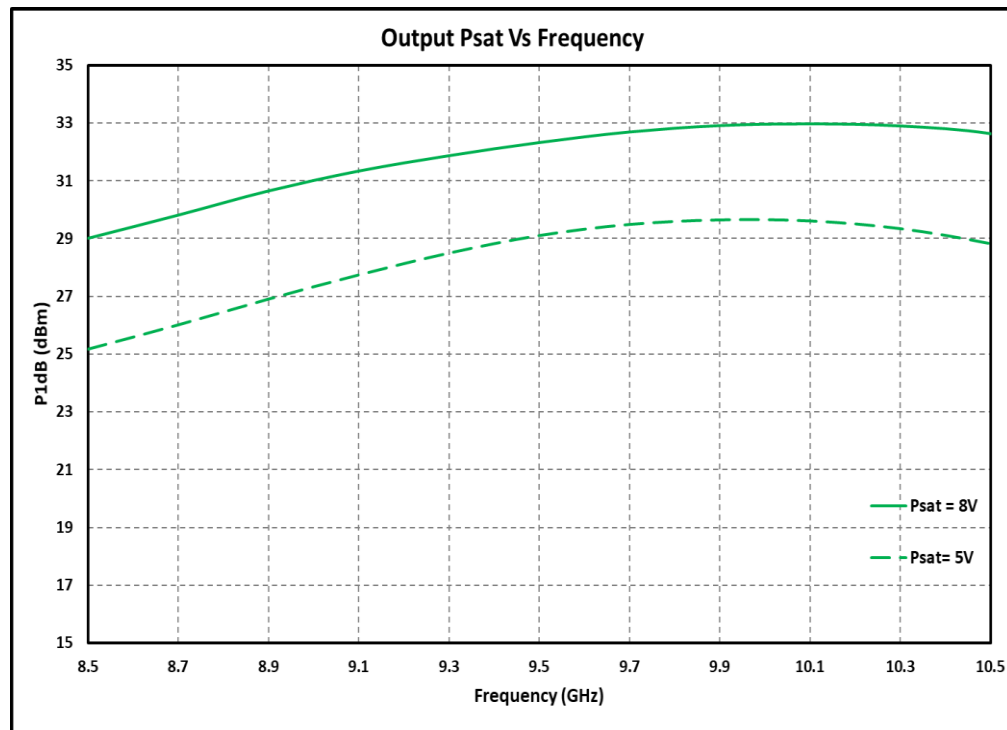
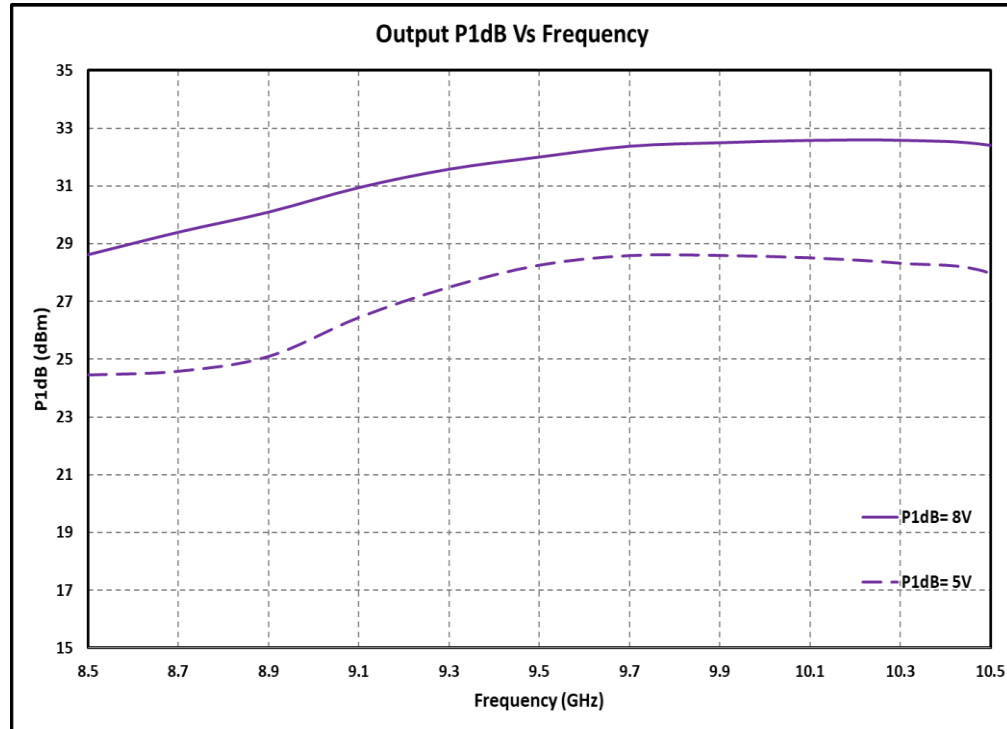
Test fixture data

$V_{d1} = V_{d2} = V_d$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



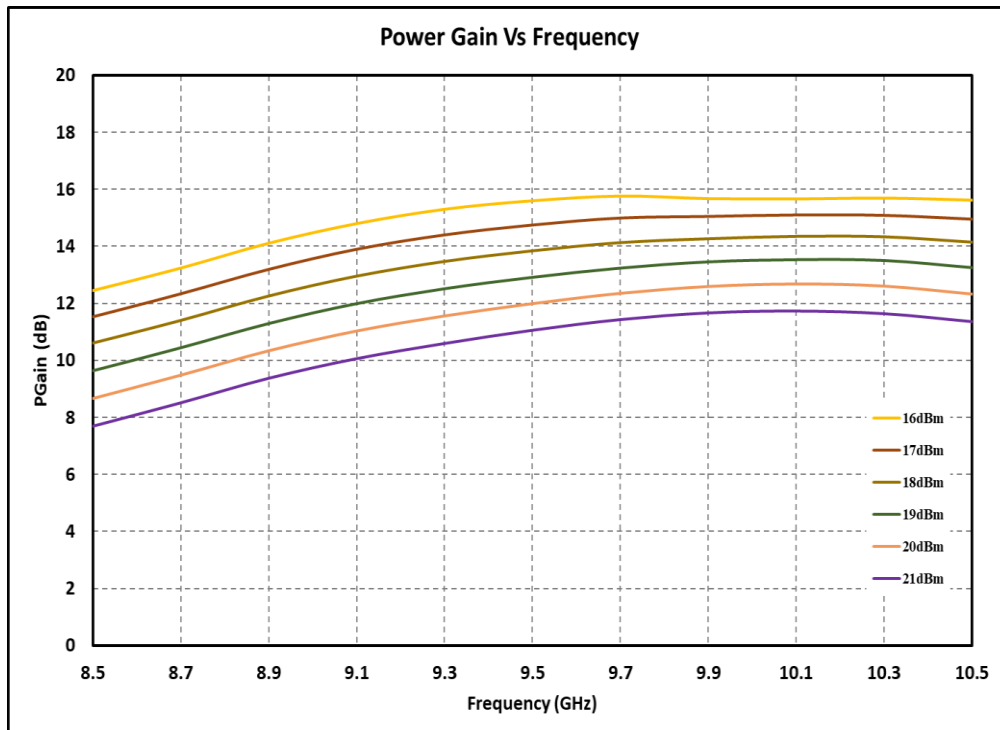
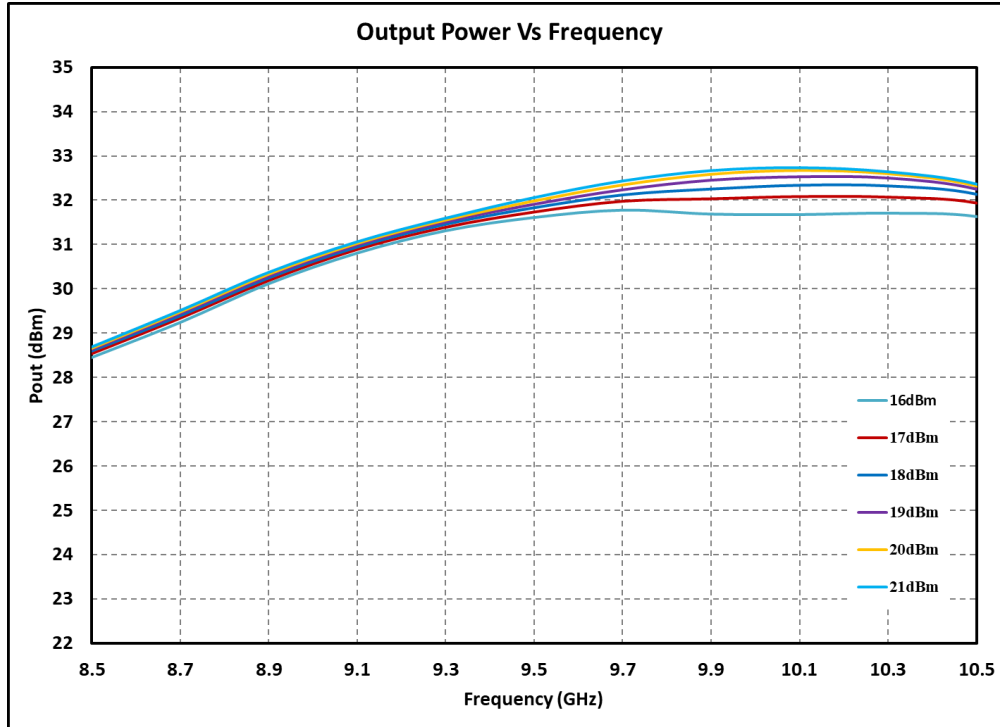
Test fixture data

$V_{d1} = V_{d2} = V_d$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



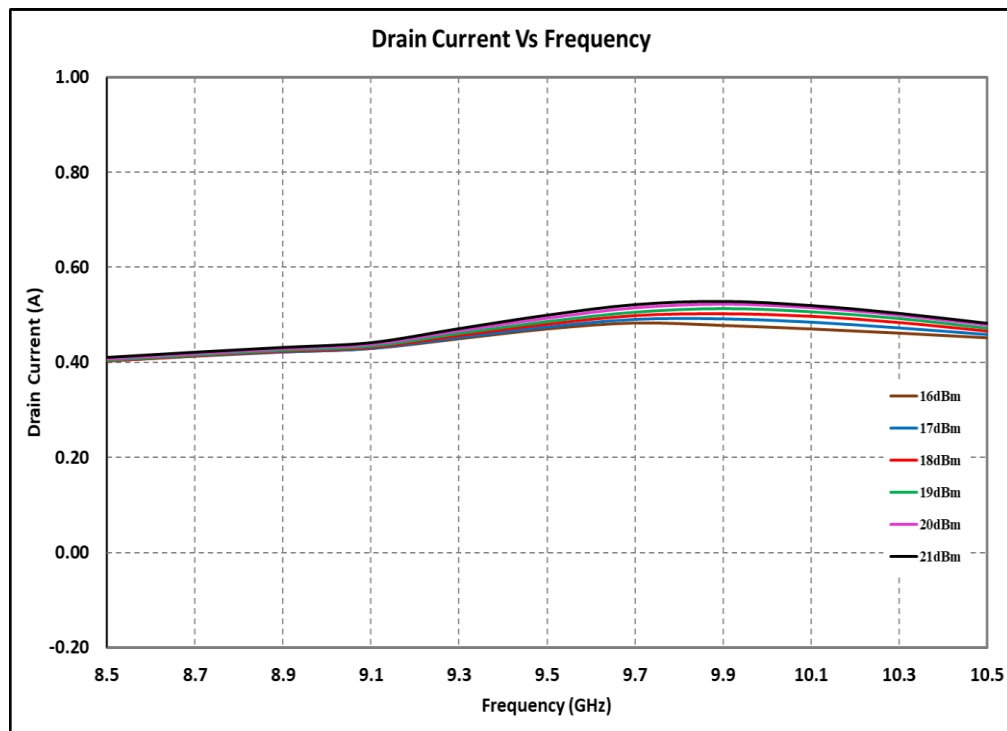
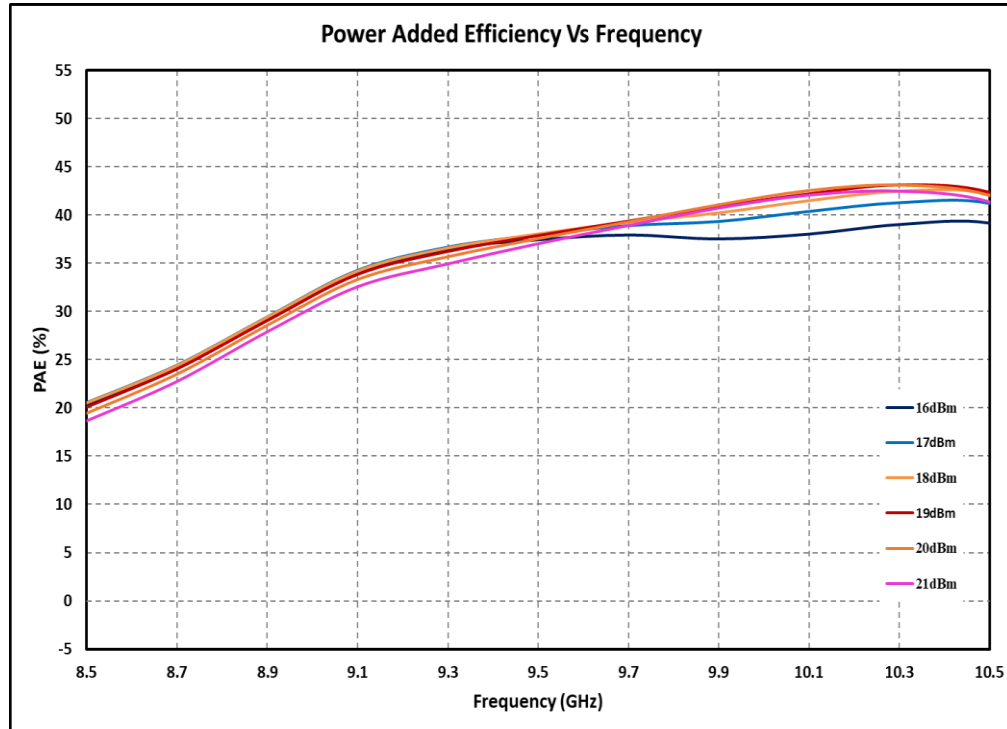
Test fixture data

$V_{d1} = V_{d2} = 8V$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



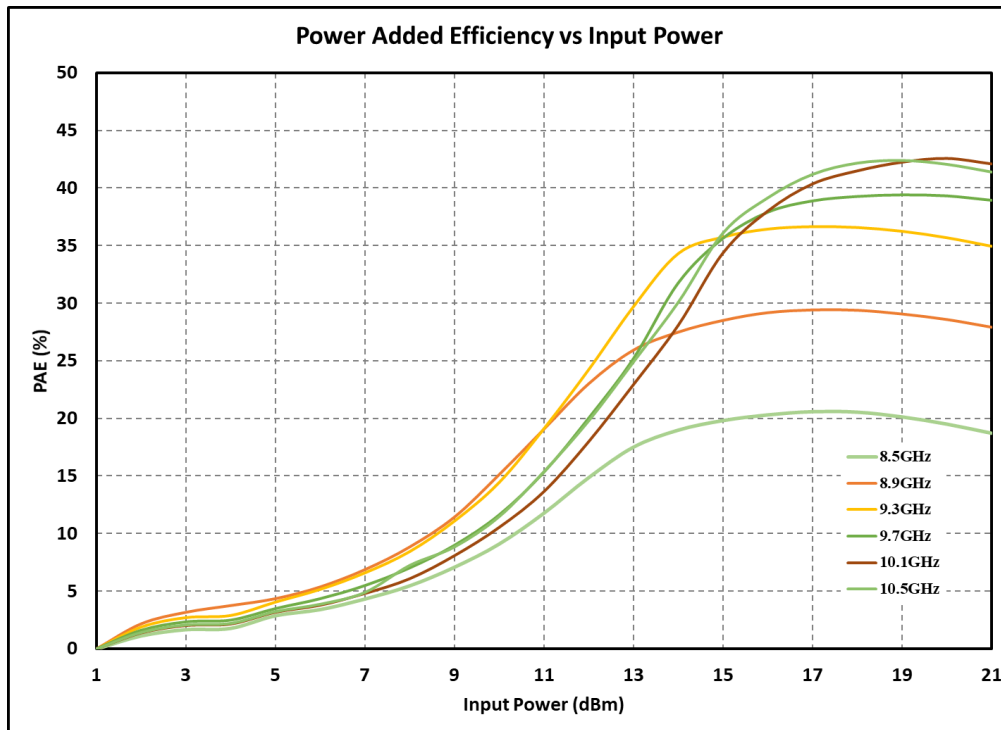
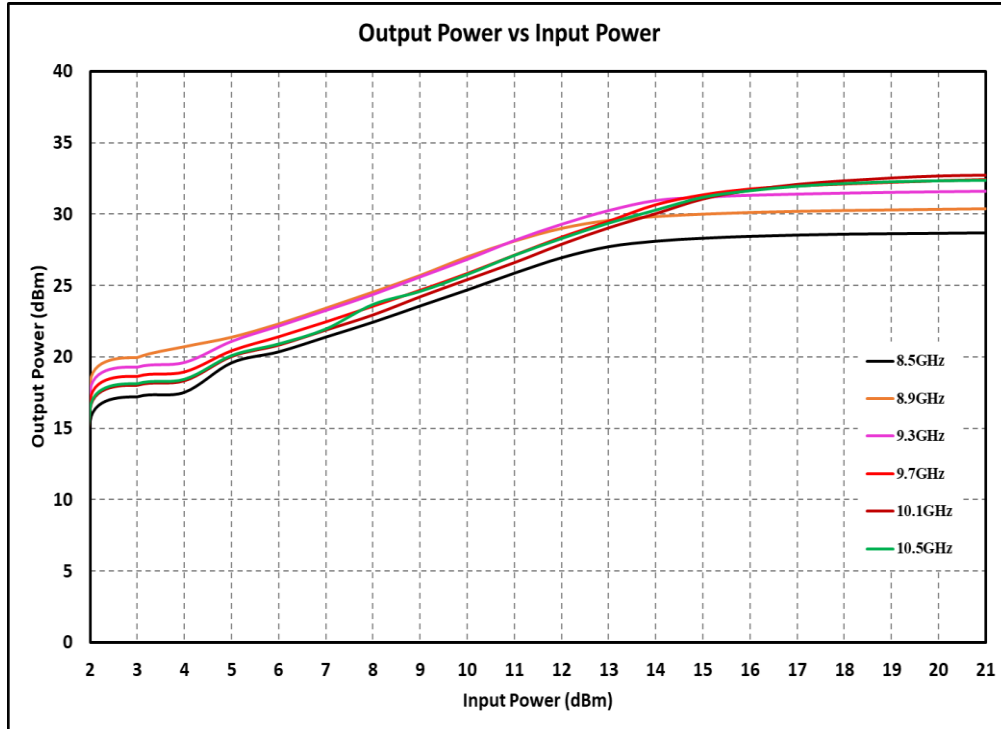
Test fixture data

$V_{d1} = V_{d2} = 8V$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



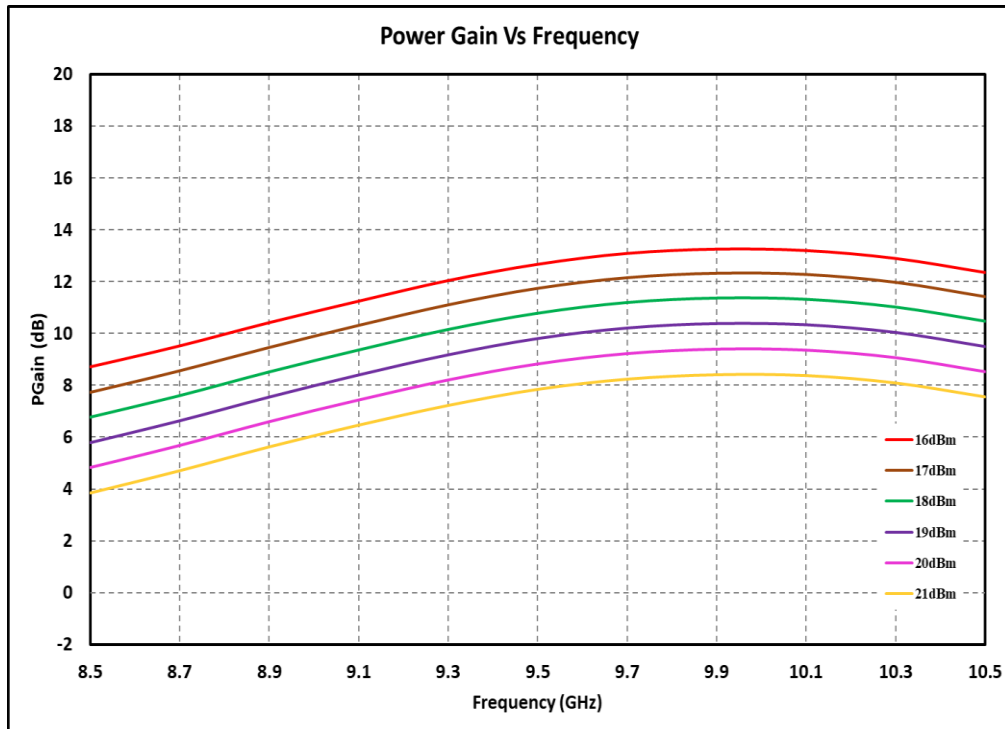
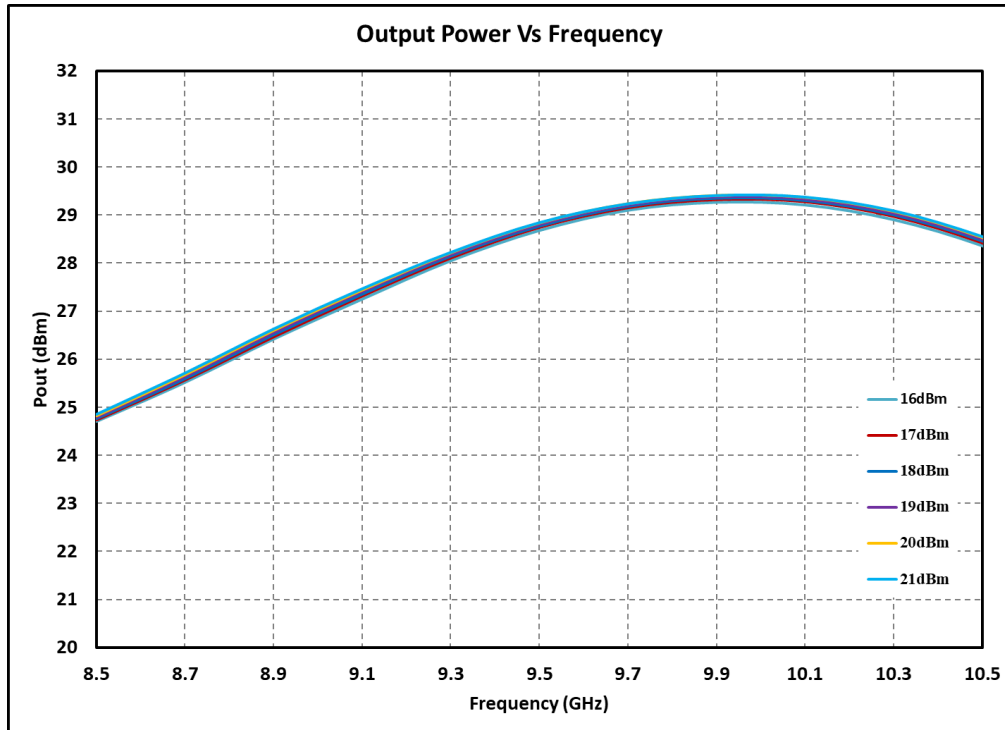
Test fixture data

$V_{d1} = V_{d2} = 8V$, $V_g = -1V$, Total Current (I_{dq}) = 370mA, $T_A = 25^\circ C$



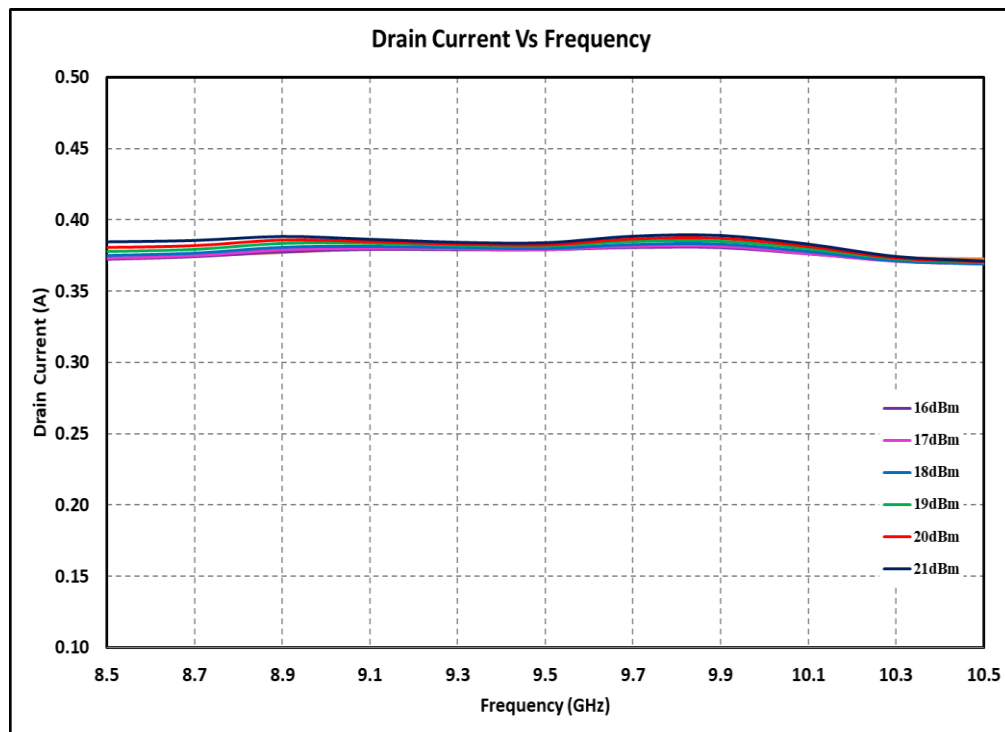
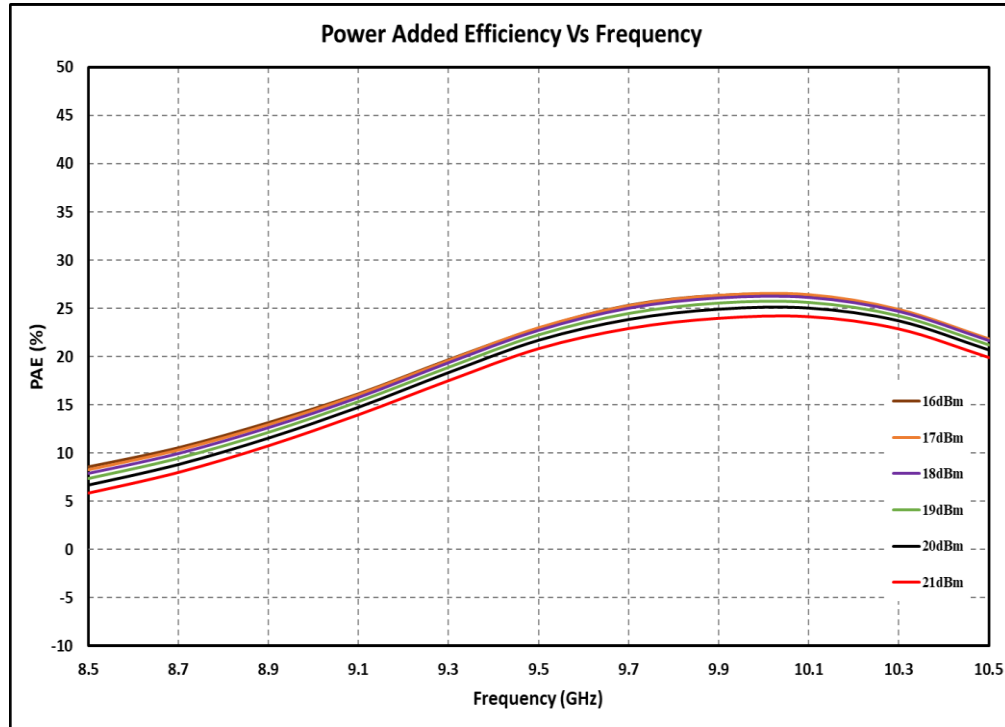
Test fixture data

$V_{d1} = V_{d2} = 5V$, $V_g = -1$, Total Current (I_{dq}) = 390mA, $T_A = 25^\circ C$



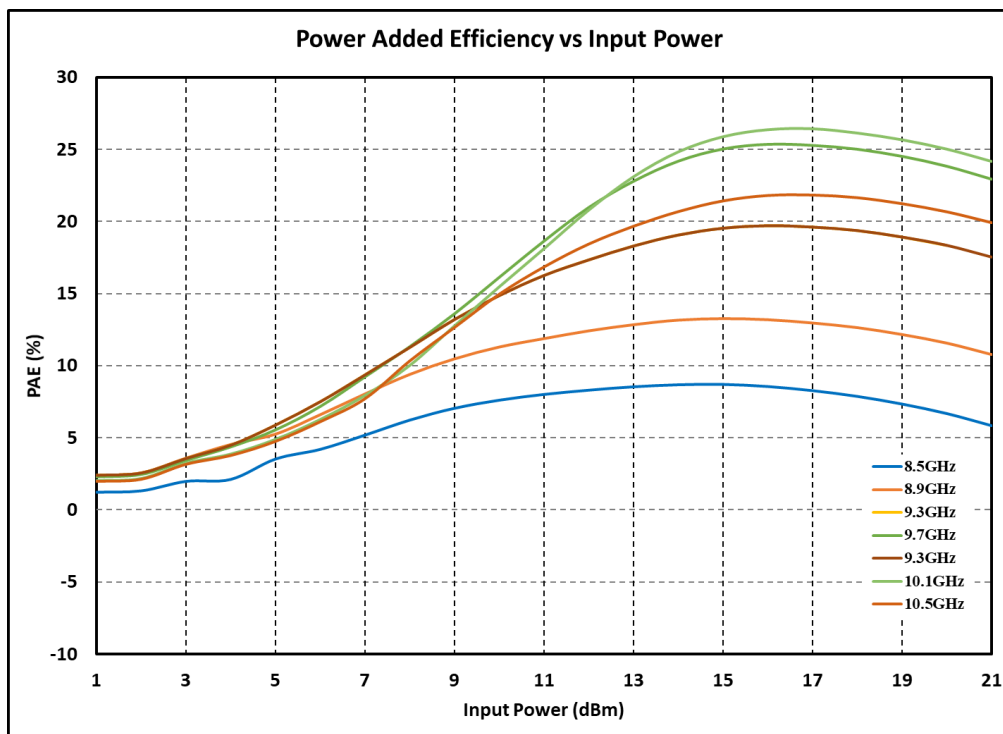
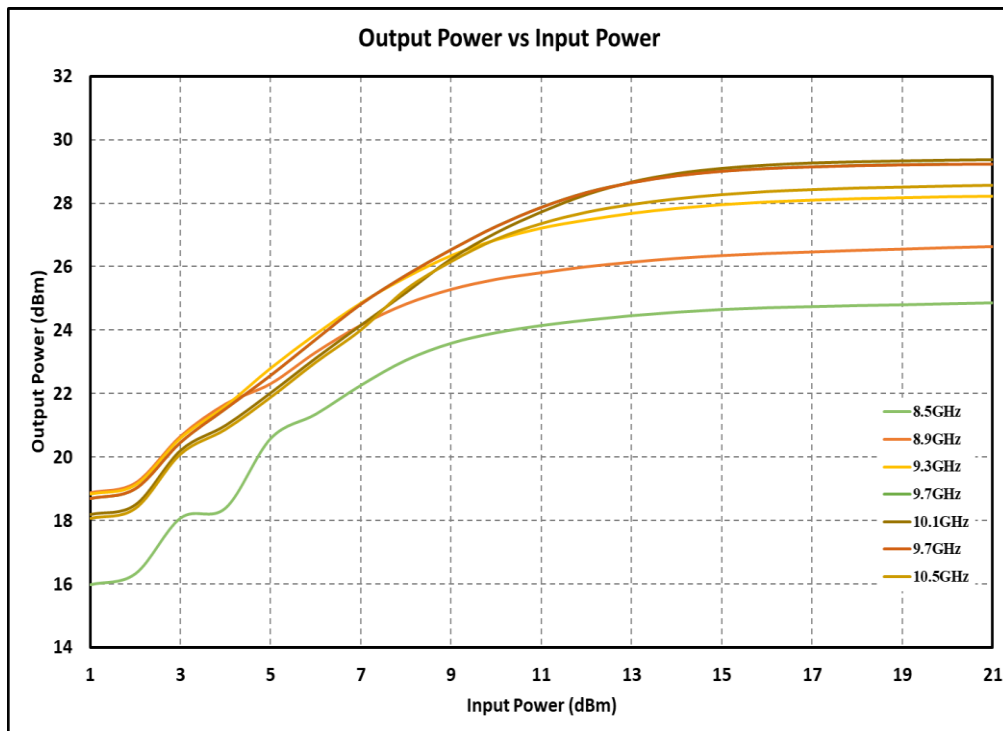
Test fixture data

$V_{d1} = V_{d2} = 5V$, $V_g = -1V$, Total Current (I_{dq}) = 390mA, $T_A = 25^\circ C$

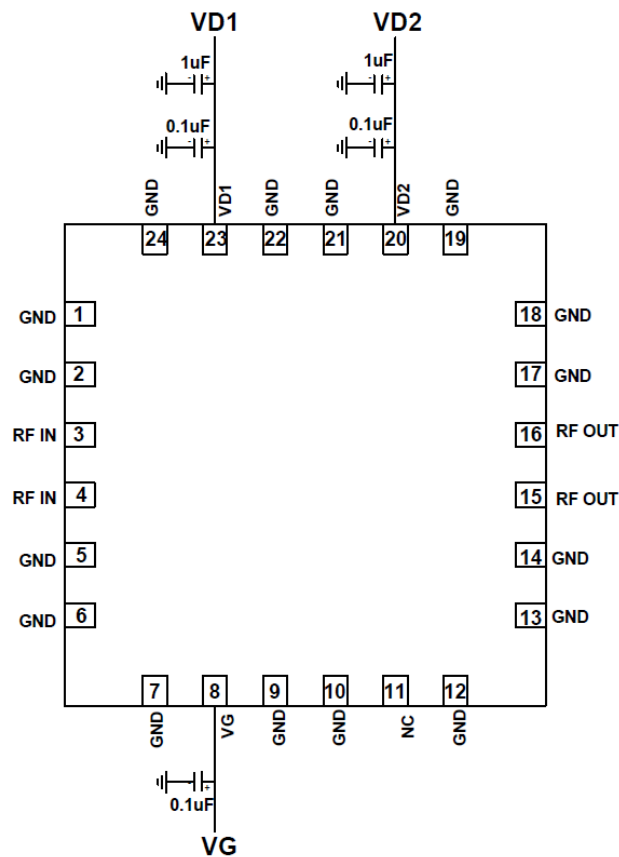


Test fixture data

$V_{d1} = V_{d2} = 5V$, $V_g = -1V$, Total Current (I_{dq}) = 390mA, $T_A = 25^\circ C$



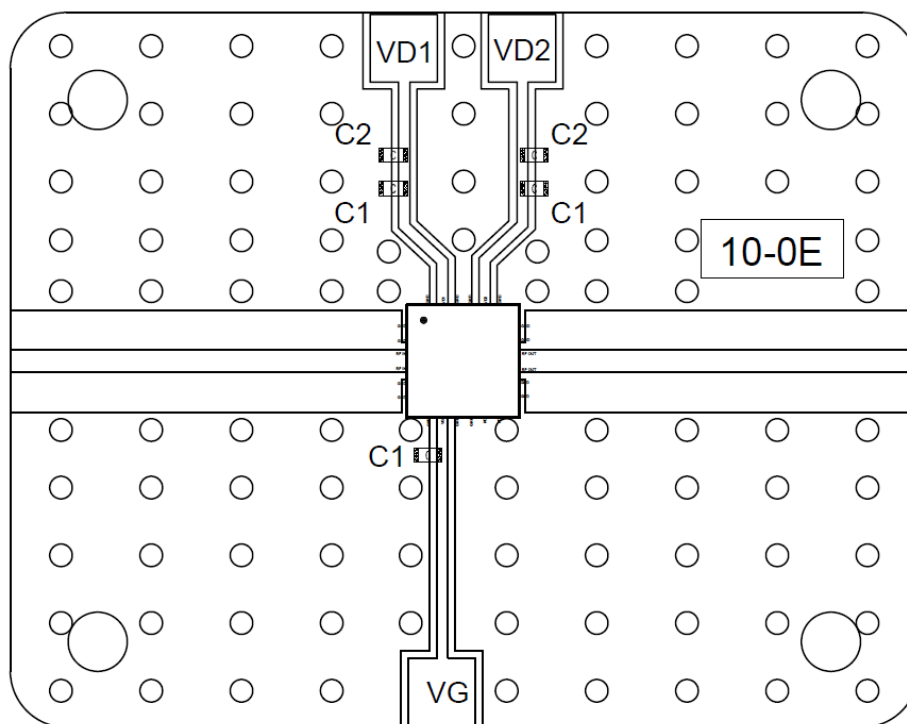
Pin Configuration & Application circuit:



Pin Description:

- | | |
|---|---|
| 1. Pin no. 3 & 4 | : RF IN (RF Input) |
| 2. Pin no. 8 | : Vg (Common gate voltage for 1 st and 2 nd Stages) |
| 3. Pin no. 23 | : Vd1 (1 st Stage Drain Voltage) |
| 4. Pin no. 20 | : Vd2 (2 nd Stage Drain Voltage) |
| 5. Pin no. 15,16 | : RF OUT (RF Output) |
| 6. Pad no. 11 | : NC (No Connection) |
| 7. Pin no. 1, 2, 5, 6, 7
9, 10, 12, 13, 14,17
18, 19, 21, 22 & 24 | : GND (Ground) |

Recommended Assembly Diagram



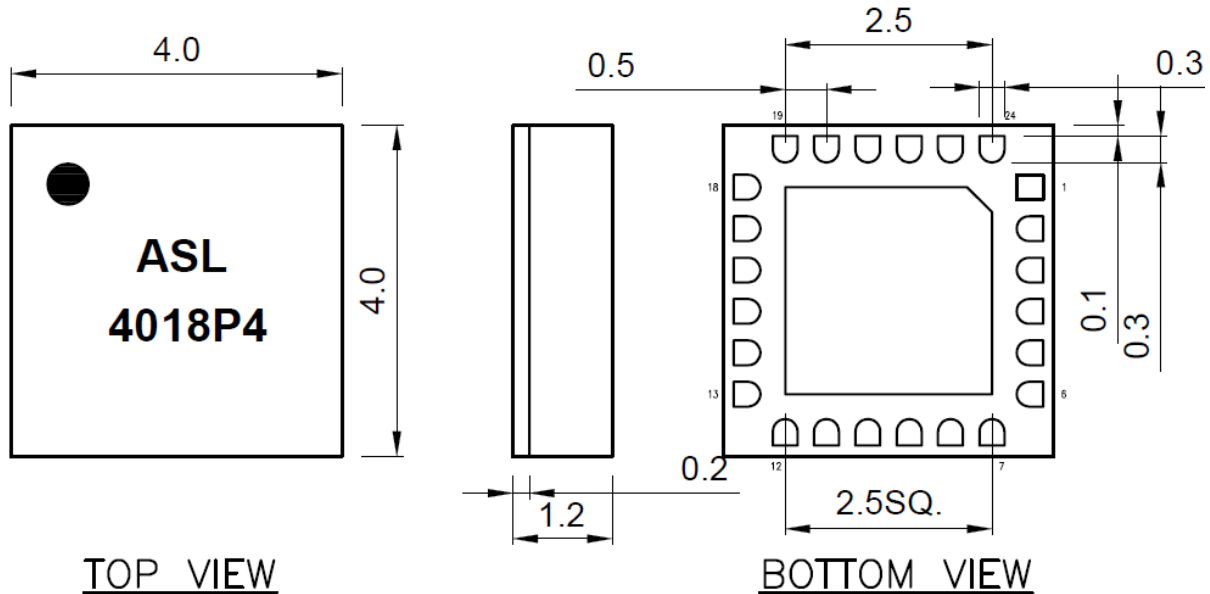
Off Chip Component Details:

Component	Part Number/Description	Vendor
0.1uF MLC (C1)	VJ0402Y102KNAAJ/1kpF±10%;25V or Equivalent	Vishay or Equivalent
1uF MLC (C2)	0402G104KXJRW1BC/1uF±10% 16V or Equivalent	Vishay or Equivalent

Note:

1. Input and output 50-ohm lines are preferably on 10 mil RT Duroid substrate.
2. Gate Bypass Capacitor "C1" and the Drain Bypass Capacitor "C2" need to be placed close to The chip.
3. Input and Output ports are DC decoupled ports.
4. Use high thermal conductive material for mounting of the chip for long-term reliability.

Package Mechanical Details:



Note:

1. Body: Ceramic Grade.
2. Lead Finish: Full Gold Plate [Gold (1-2um) on Nickel (2.5-7.6um) Plating].
3. All Dimension mentioned are in mm (millimeters).



GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice. Before using the product, please download and refer to datasheet from website.