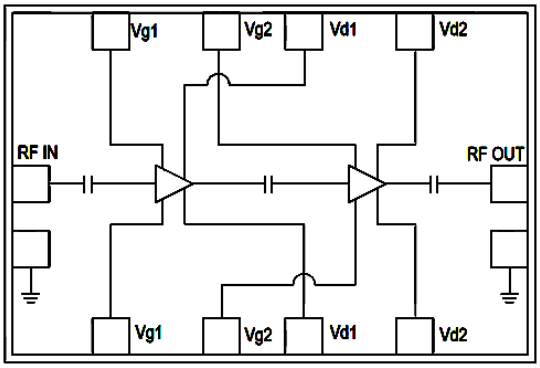
8.5 – 10 GHz 5 Watt Power Amplifier

Features

- **Frequency Range : 8.5 – 10GHz**
- **37.5 dBm Psat**
- **23 dB Power gain**
- **38% PAE**
- **High IP3**
- **Dual bias operation**
- **DC decoupled input and output**
- **On Chip Power Detector**
- **0.25 µm InGaAs pHEMT Technology**
- **Chip dimension: 4.8 x 2.15 x 0.1 mm**

Functional Drawing



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4043 is an X-band Power amplifier with 37.5dBm power output. The PA uses 2 stages of amplification and operates in 8.5 – 10 GHz frequency range. The PA features 23 dB of gain with small signal input and output return losses of 9 dB respectively. The PA has a high IP3 of 46dBm and 38% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.25µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+8.5	volts
Drain current (Id)	2.5	A
RF input power (RFin at Vd=8V)	20	dBm
Operating temperature	-50 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.8V
Z_o =50 Ω, Pulse Duty Cycle = 10%

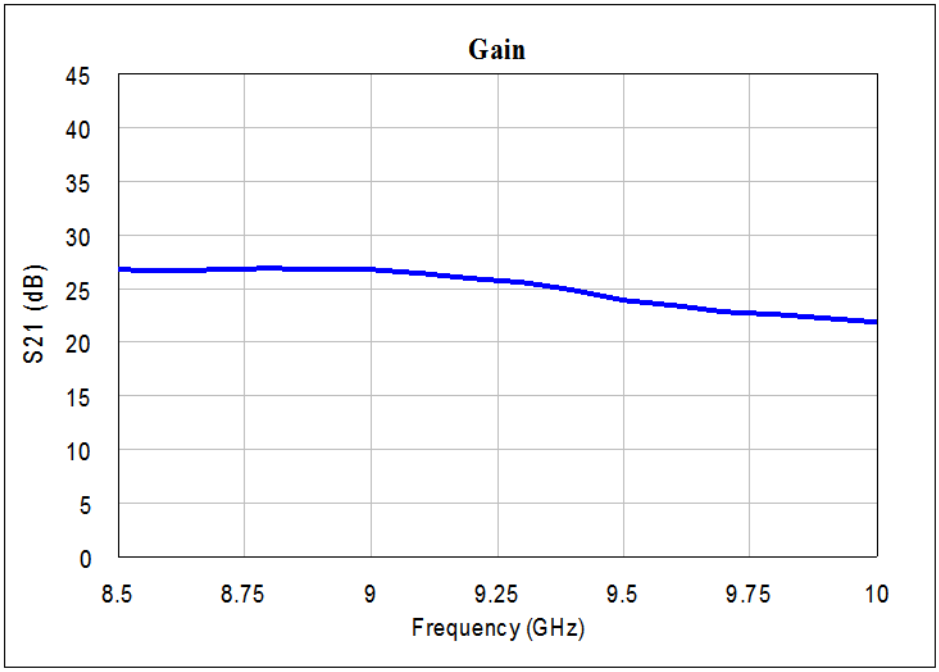
Parameter	Typ.	Units
Frequency Range	8.5 – 10	GHz
Gain	23	dB
Gain Flatness	+/-1.9	dB
Output Power (P1 dB)	36.5	dBm
Input Return Loss	9	dB
Output Return Loss	9	dB
Saturated output power (Psat)	37.5	dBm
Output Third Order Intercept (IP3)	46	dBm
Power Added Efficiency (PAE)	38%	--
Supply Current(I_{dq})	1.4	A
Supply Current(I_{dsat}^2)	1.95	A

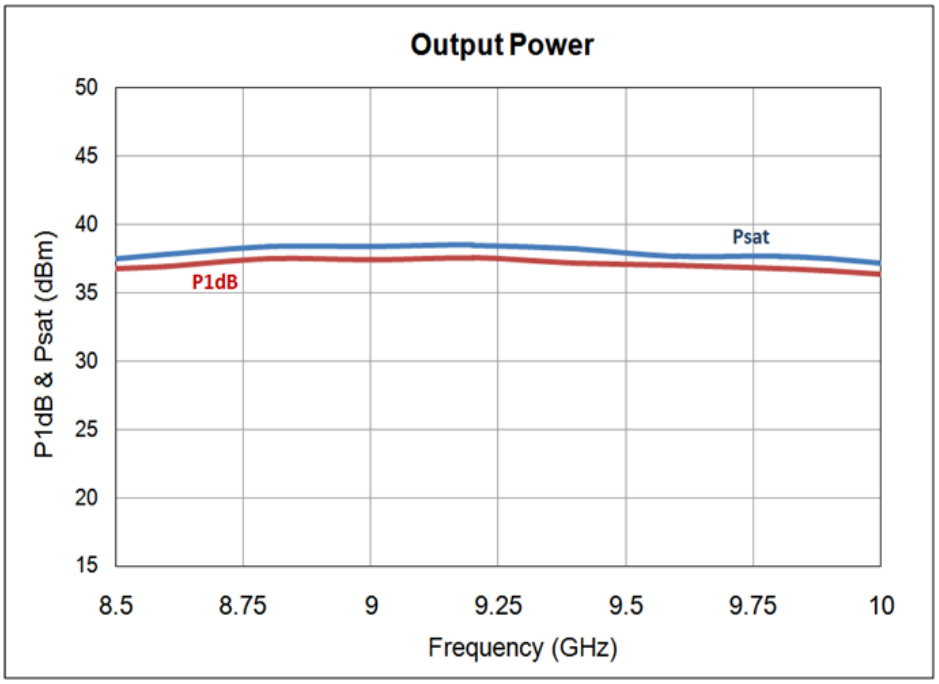
Note:

1. Electrical specifications as measured in test fixture.
2. I_{dsat} is the drain current corresponding to saturated output power.

Test fixture data

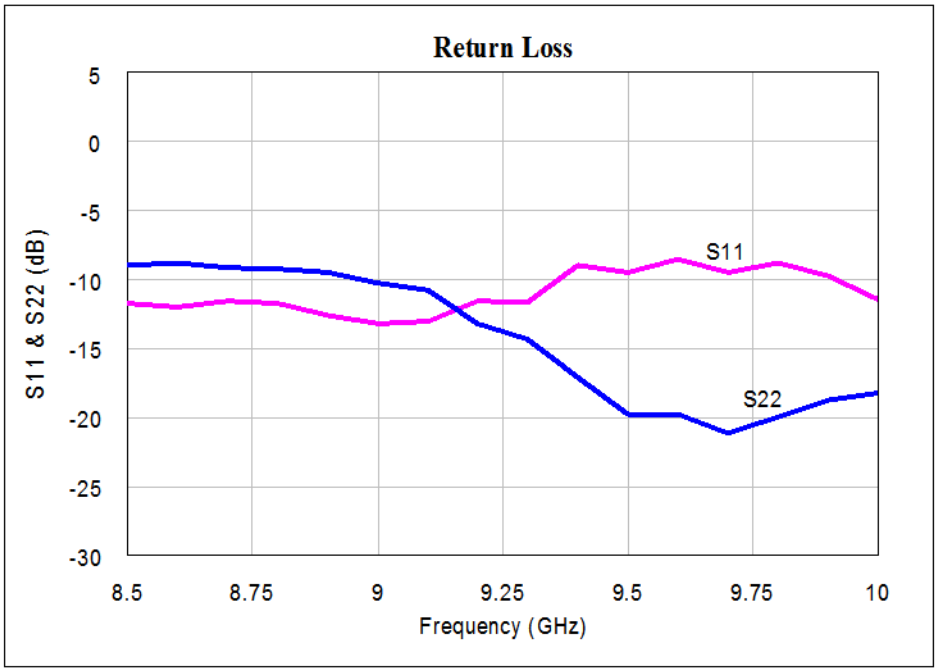
V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.8V, Total Current (Idq) =1.4A, T_A = 25 ^oC, Pulse Duty Cycle = 10%

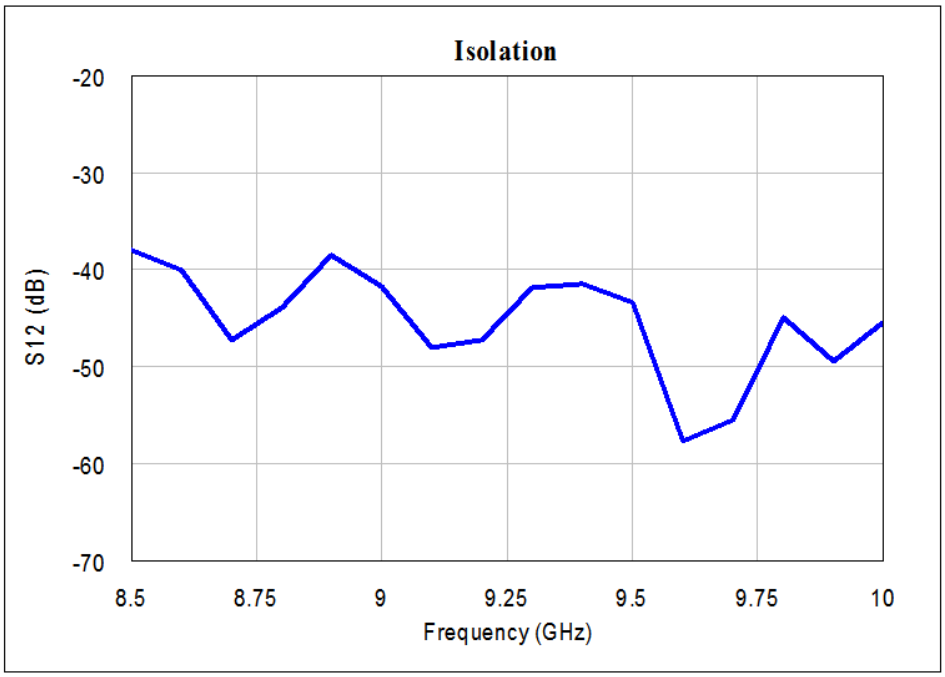




Test fixture data

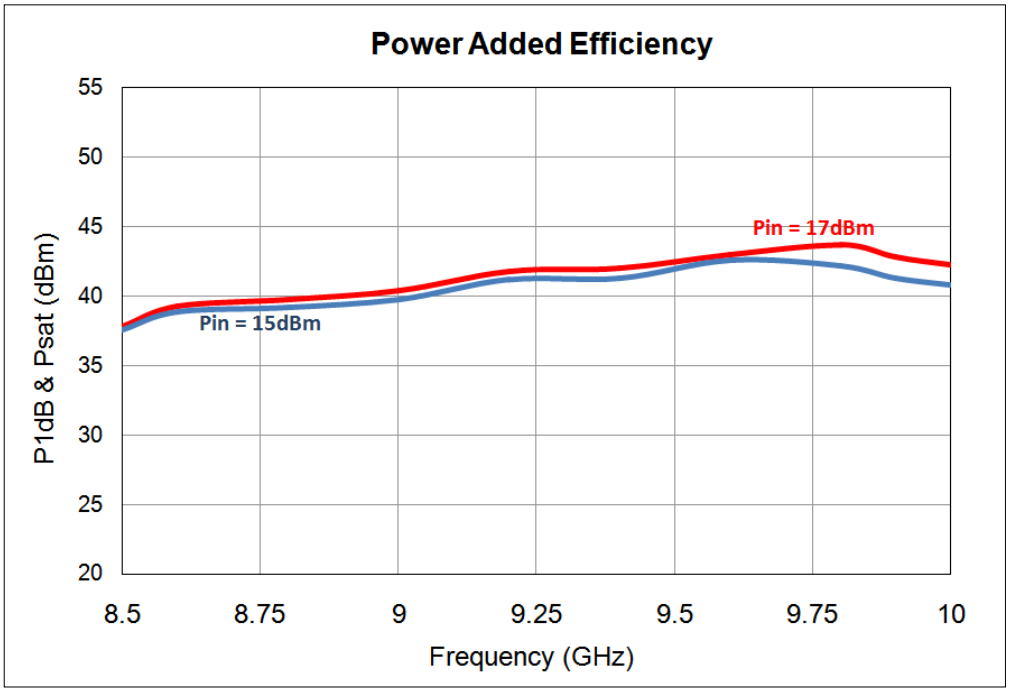
V_{d1} = V_{d2} = 8V, *V_{g1} = V_{g2} = -0.8V, Total Current (Idq) =1.4A, T_A = 25 ^oC, Pulse Duty Cycle = 10%*

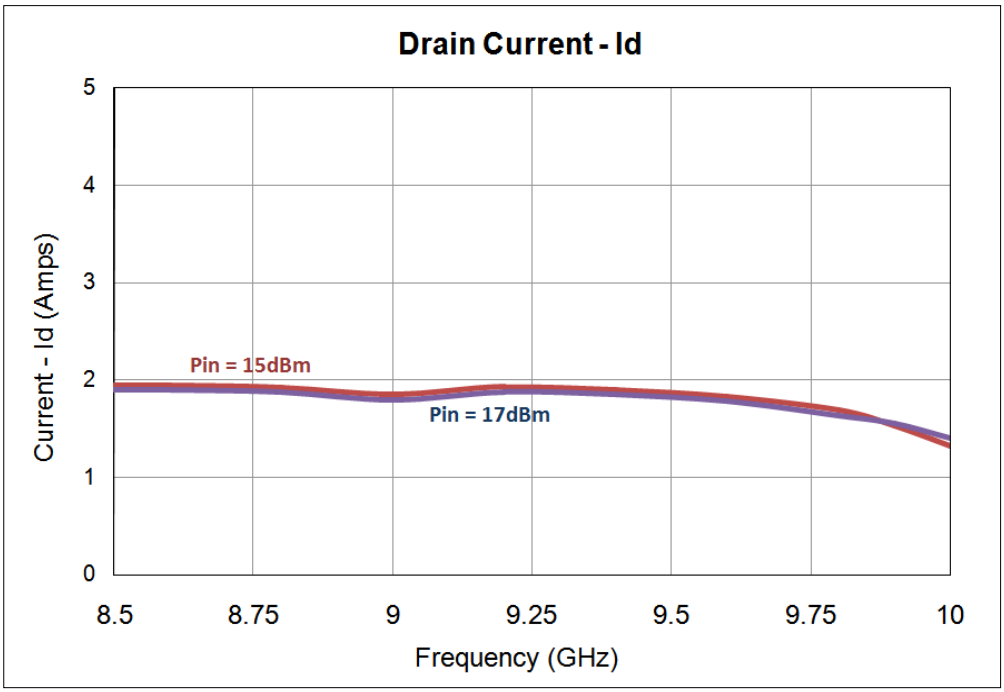




Test fixture data

V_{d1} = V_{d2} = 8V, *V_{g1} = V_{g2} = -0.8V, Total Current (Idq) =1.4A, T_A = 25 ^{o}C, Pulse Duty Cycle = 10%*





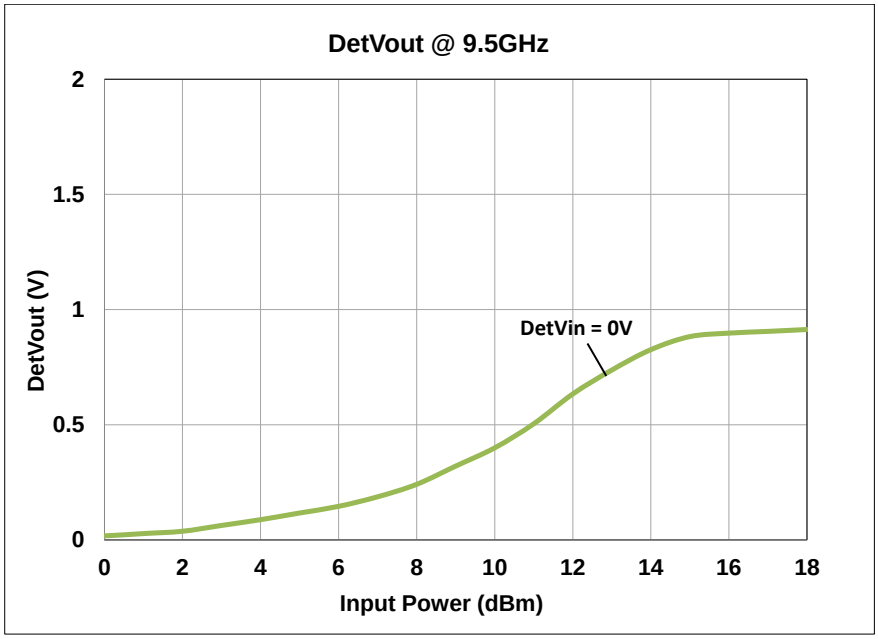
Power Detector Performance:

Test fixture data

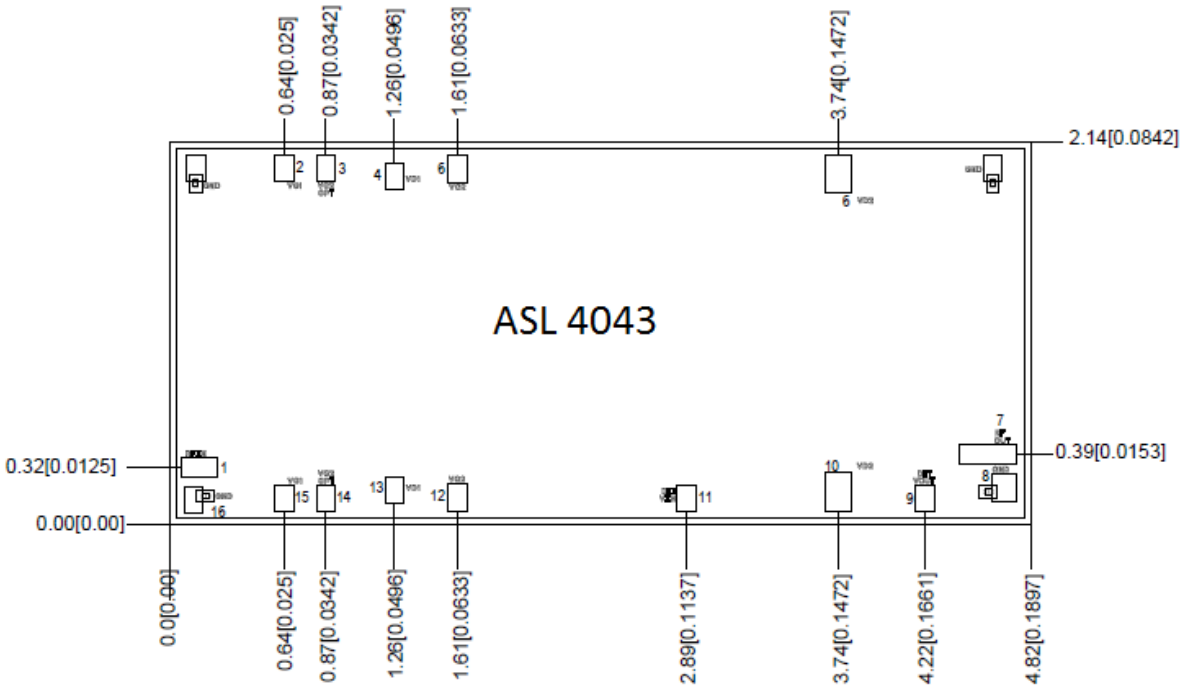
V_{d1} = V_{d2} = 8V, *V_{g1} = V_{g2} = -0.8V, Total Current (Idq) =1.4A, T_A = 25 ^oC, DetVin = 8V, Pulse Duty Cycle = 10%*

Pout (dBm)	9GHz	9.5GHz	10GHz
37dBm	DetVout = 0.95V	DetVout = 0.9V	DetVout = 0.8V
-30dBm	DetVout = 0V	DetVout = 0V	DetVout = 0V

Description: The Output Voltage of the detector ”DetVout” increases with increase in RF output power of the power amplifier. The On Chip Detector can be operated by connecting its input terminal ”DetVin” to ground and the output of the detector is tapped from ”DetVout”.
The performance of the detector with respect to variation of input power of the PA at 9.5GHz is plotted below.



Bond Pad Locations

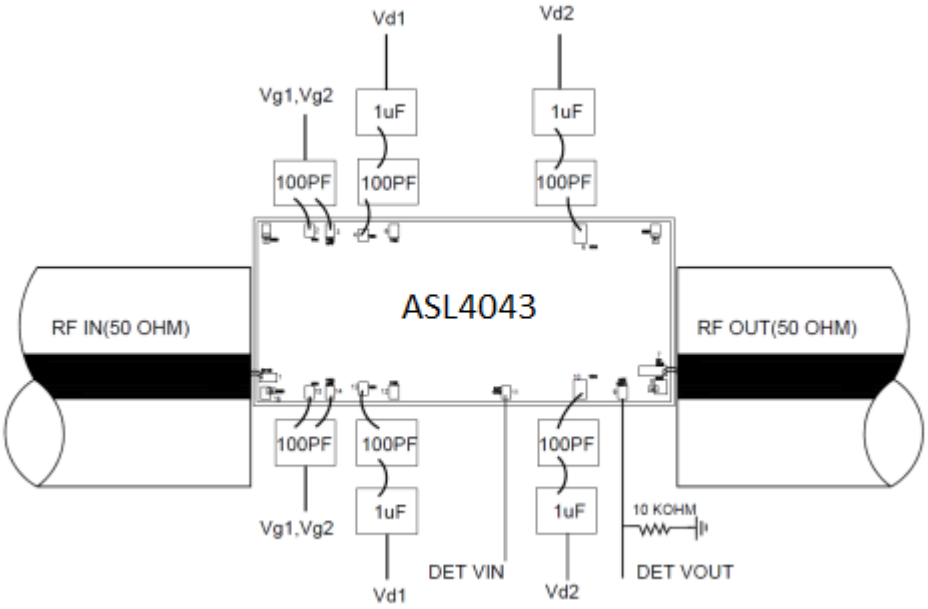


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 2,15 : 1st stage gate voltage(V_{g1})
4. Pad no. 7 : RF Output
5. Pad no. 4,13 : 1st stage drain voltage(V_{d1})
6. Pad no. 3,14 : 2nd stage gate voltage(V_{g2})
7. Pad no. 6,10 : 2nd stage drain voltage (V_{d2})
8. Pad no. 11 : Input Voltage for Power Detector (DetVin)
9. Pad no. 9 : Output Voltage for Power Detector (DetVout)
10. All the dimensions shown above are measured taking bottom left corner as reference.

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate.
4. 100pF(Single Layer) and 1uF bypass capacitors are used as shown above.
5. The RF input & output ports are DC decoupled on-chip.
6. This chip is not preferred to be operated under continuous DC voltage, unless it is applied with considerably low drain voltage level.
7. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip

Die attach: Eutectic attachment using fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice